


SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER STATES

Voltage	Description	Control Signal	SLP_S5#	SLP_S4#	SLP_S3#
PWR_SRC	AC ADAPTER OR BATTERY IN		HIGH	HIGH	HIGH
+5VALW	5.0V always on power rail	PWR_SRC	ON	ON	ON
+3VALW	3.3V always on power rail	PWR_SRC	ON	ON	ON
+5VSUS	5.0V power rail	SUS_ON	ON	ON	ON
+3VSUS	3.3V power rail	SUS_ON	ON	ON	ON
+1_8VSUS	1.8V power rail	3V5VSUSPWRGD	ON	ON	ON
+1VSUS	1.0V power rail	1_8VSUSPWRGD	ON	ON	ON
+2_5VMEM_VPP	2.5V power rail DDR (off in S4-S5)	DIMM_ON_VPP	OFF	ON	ON
+VCCST	1.0V power rail CPU (off in S4-S5)	DIMM_ON_VPP	OFF	ON	ON
+VCCPLL	1.0V power rail CPU (off in S4-S5)	+VCCST	OFF	ON	ON
+1_2VDIMM	1.2V power rail DDR (off in S4-S5)	DIMM_ON_VDDQ	OFF	ON	ON
+VDDQC	1.2V power rail CPU DRAM (off in S4-S5)	+1_2VDIMM	OFF	ON	ON
+VCCPLL_OC	1.2V power rail CPU (off in S4-S5)	+1_2VDIMM	OFF	ON	ON
+5VRUN	5.0V switched power rail (off in S3-S5)	RUND	OFF	OFF	ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUND	OFF	OFF	ON
+1_8VRUN	1.8V power rail AUDIO (off in S3-S5)	RUND	OFF	OFF	ON
+VCC_IO	1.0V rail for Processor & PCH (off in S3-S5)	RUND	OFF	OFF	ON
+VCCSTG	1.0V power rail CPU (off in S3-S5)	+VCC_IO	OFF	OFF	ON
+0_6VTT_RUN	0.6V DDR Termination voltage (off in S3-S5)	DDR_VTT_CTRL	OFF	OFF	ON
+VCC_SA	0.55V to 1.15V Voltage for Processor	VR_ON	OFF	OFF	ON
+VCC_CORE	0.55V to 1.5V Voltage for Processor	VR_ON	OFF	OFF	ON
+VCC_GT	0.55V to 1.52V Core Voltage for Processor	VR_ON	OFF	OFF	ON

Note: WHEN AC MODE, System turn on then +*VSUS will always keep high
S4 (Suspend to Disk)
S3 (Suspend to RAM)
S0 (Full ON)

 MICRO-STAR INT'L CO.,LTD.

Title

PLATFORM

Size

Document Number

Custom

MS-14B2

Date

Monday, May 28, 2018

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of

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Rev

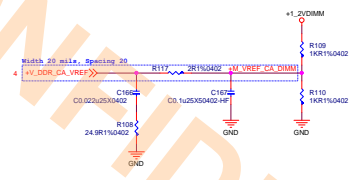
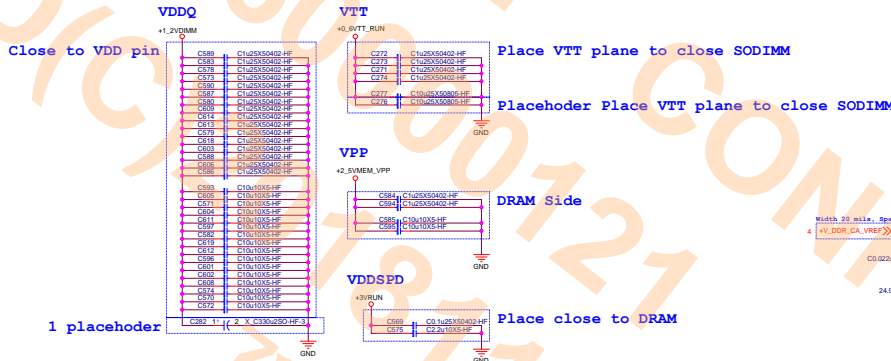
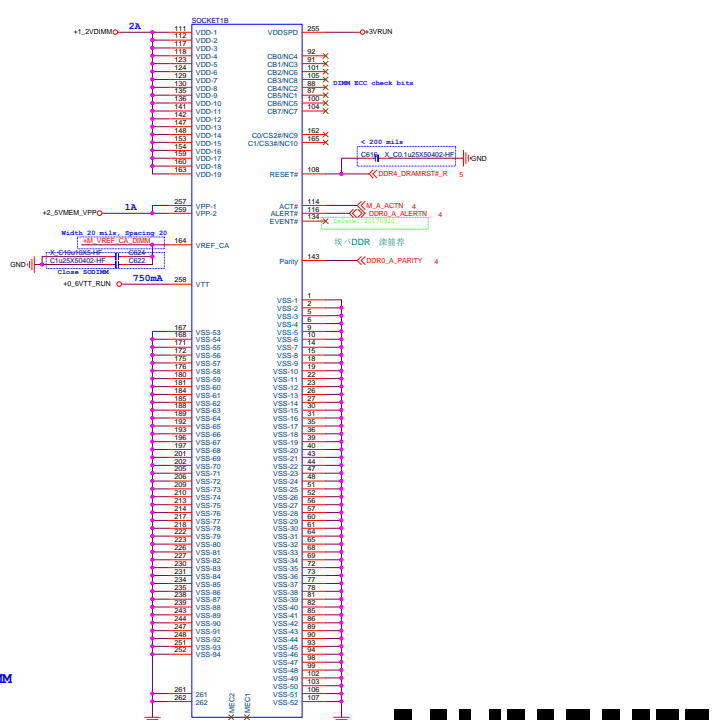
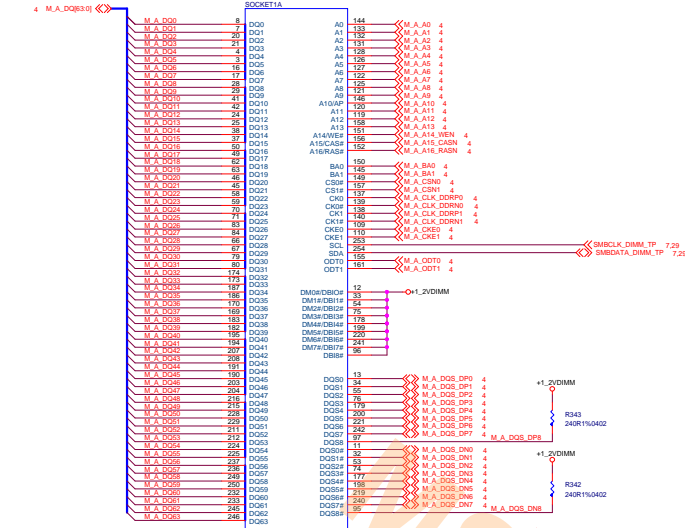
10

8111520001 weilu(盧偉) 客戶服務部

KBL_R_U42_1P0_IP
BGA1356

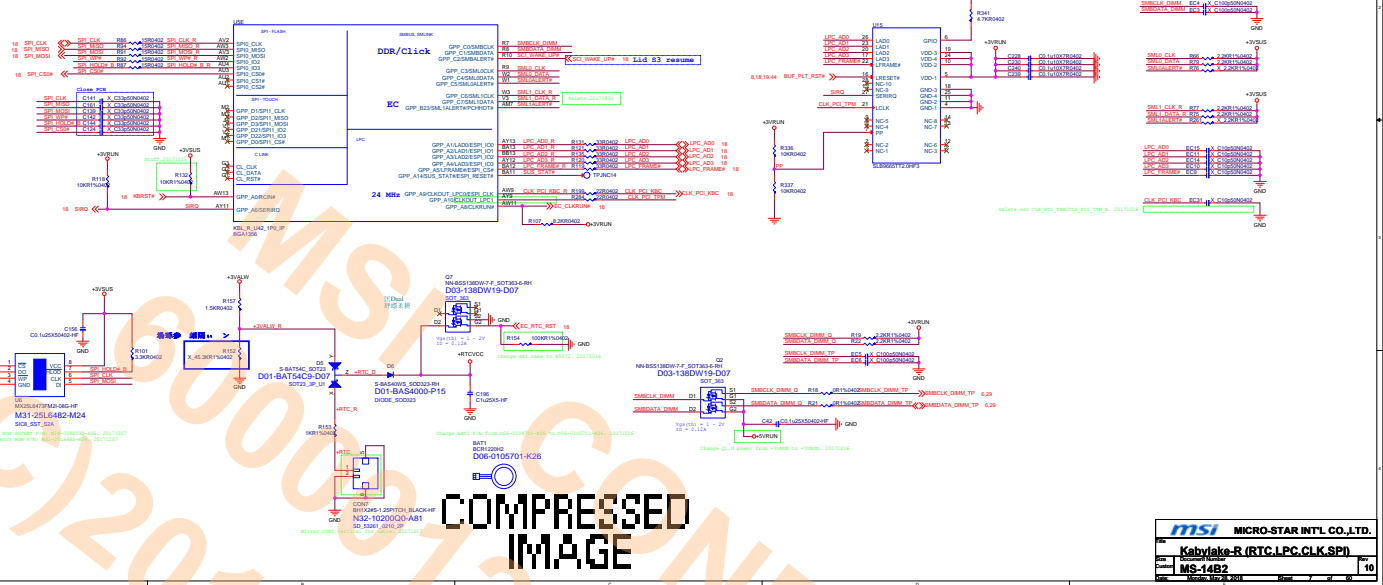


SODIMM_A (Bottom)

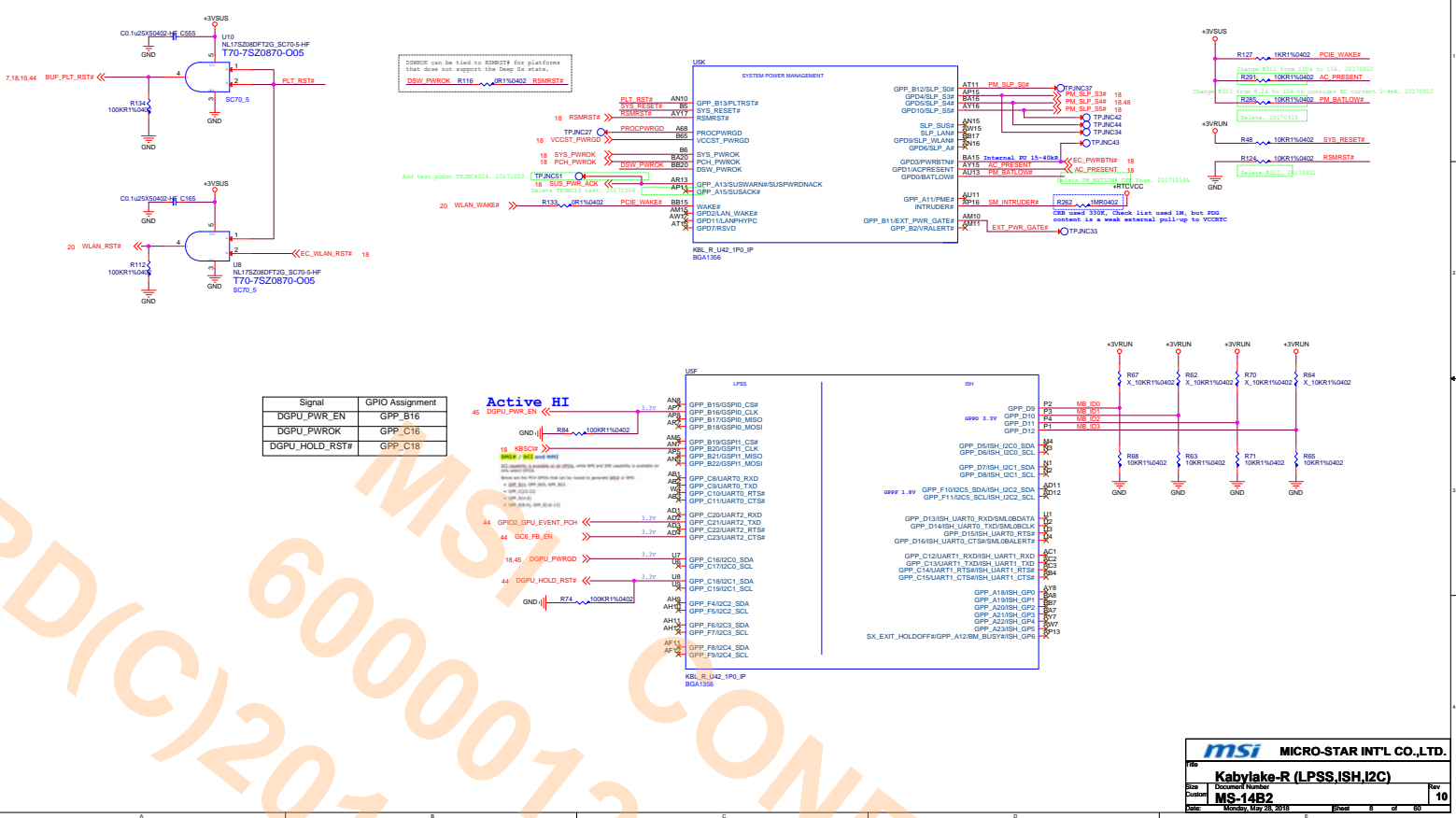


COMPRESSED
IMAGE

COMPRESSED IMAGE COMPRESSED IMAGE COMPRESSED IMAGE



msi MICRO-STAR INT'L CO.,LTD.	
Kabylake-R (RTC,LPC,CLK,SPi)	
MS-14B2	10

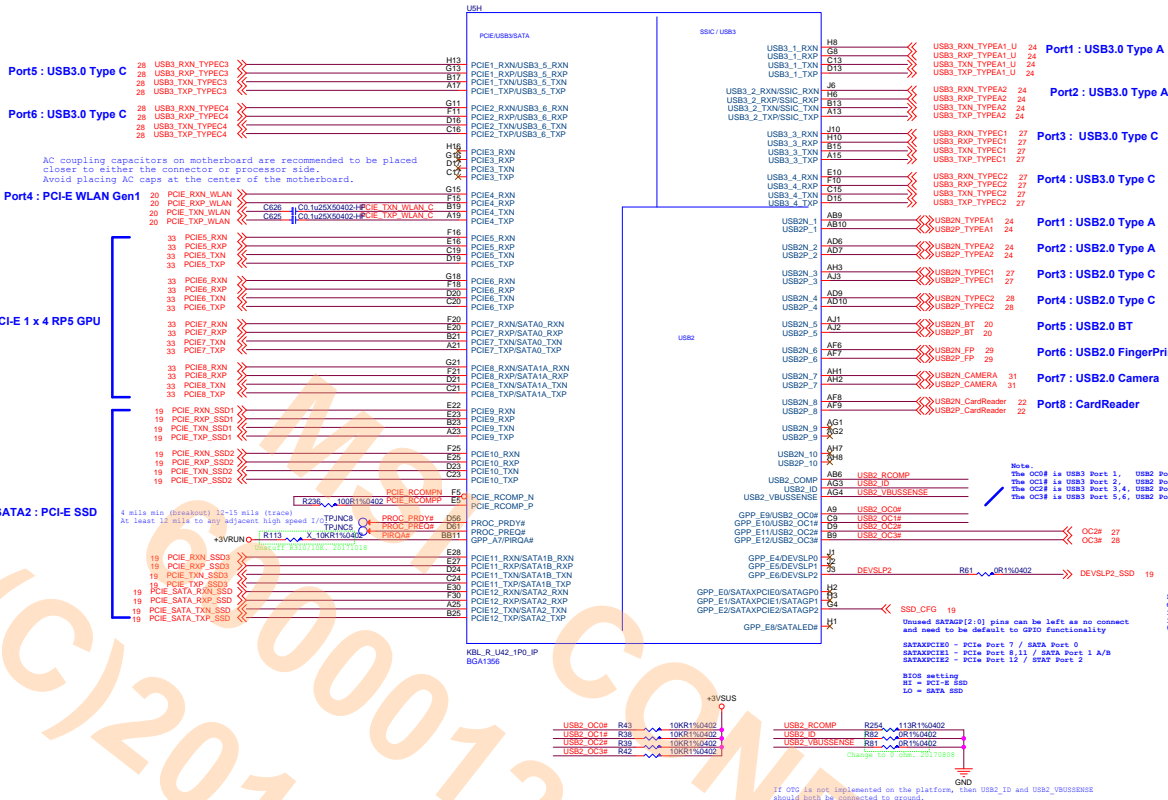


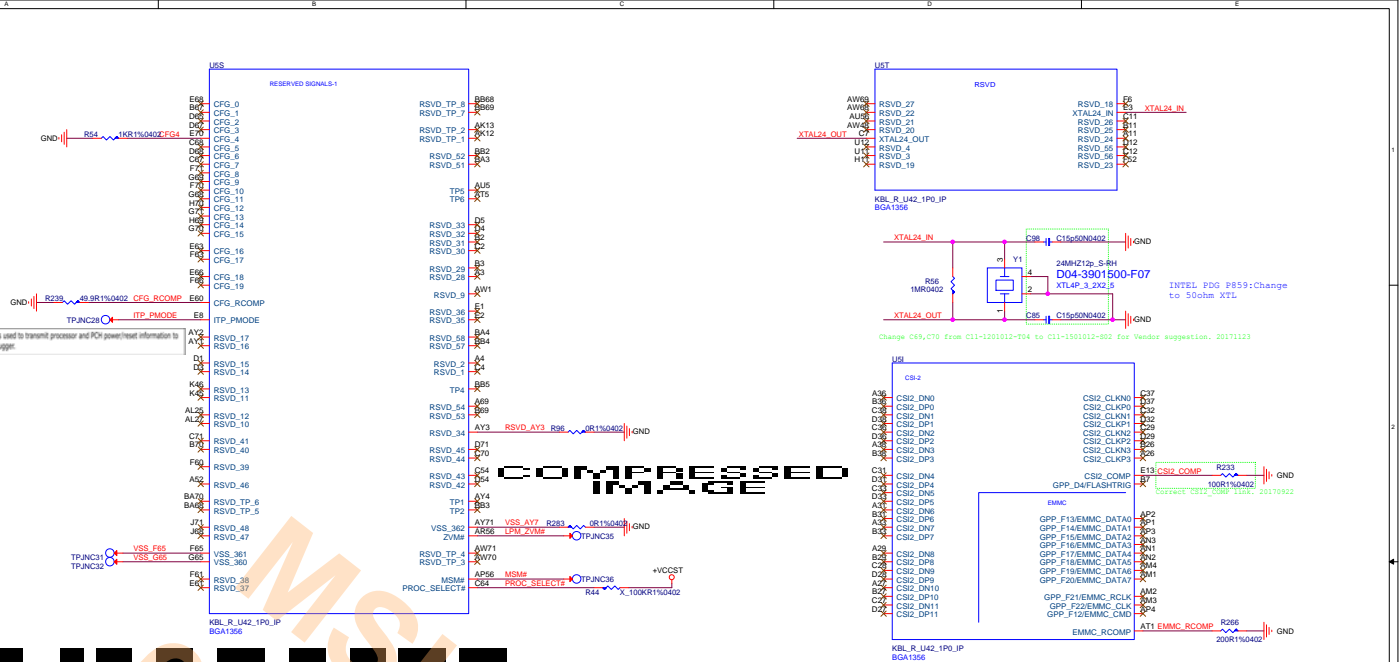
Signal	GPIO Assignment
DGPU_PWR_EN	GPIO_B16
DGPU_PWR_OK	GPIO_C16
DGPU_HOLD_RST#	GPIO_C18

Active HI

MICRO-STAR INT'L CO.,LTD.

File	Kabylake-R (LPSS,ISH,I2C)		Rev
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Processor Select: This pin is for compatibility with future platforms. It should be unconnected for the processor.

All the RSVD pins should be left unconnected (floating) on the board.

Name	Type	Description
CSI2_DP[11:0]	I	MIPI CSI-2 Data
CSI2_DN[11:0]	I	MIPI CSI-2 Data
CSI2_CLKP[3:0]	I	MIPI CSI-2 Clock
CSI2_CLKN[3:0]	I	MIPI CSI-2 Clock
CSI2_COMP	I	External Reference (100 Ohm +/- 1% pull down to ground)

Name	Type	Description
EMMC_CMD	I/O	eMMC Command/Response
EMMC_DATA0	I/O	eMMC Data
EMMC_DATA1	I/O	eMMC Data
EMMC_DATA2	I/O	eMMC Data
EMMC_DATA3	I/O	eMMC Data
EMMC_DATA4	I/O	eMMC Data
EMMC_DATA5	I/O	eMMC Data
EMMC_DATA6	I/O	eMMC Data
EMMC_DATA7	I/O	eMMC Data
EMMC_RCLK	I	eMMC Receive Clock
EMMC_CLK	O	eMMC Clock
EMMC_RCOMP	I/O	External reference (200 Ohm +/- 1% pull down to ground)

msi MICRO-STAR INT'L CO.,LTD.

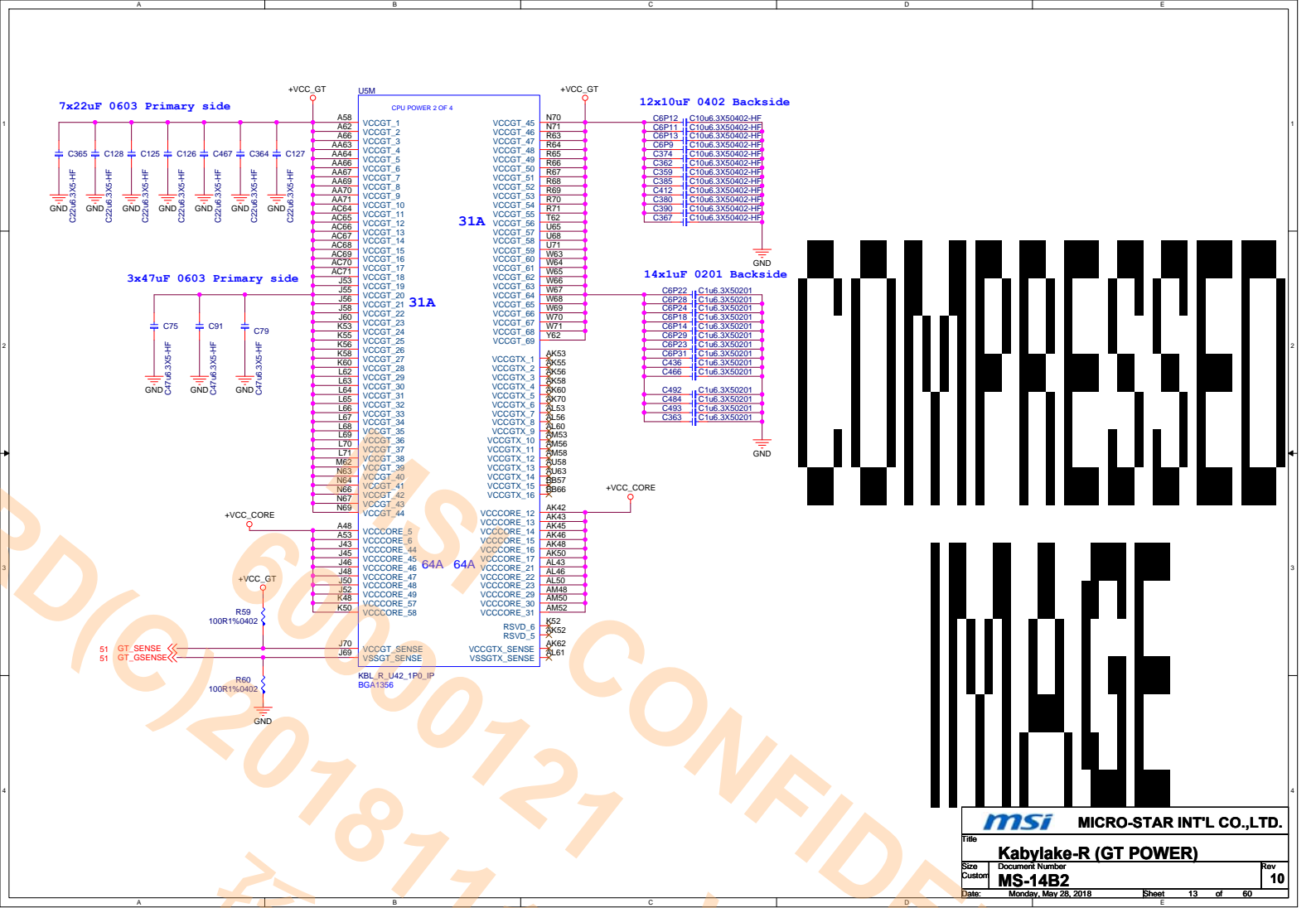
KabyLake-R (CFG,CSI,RSVD)

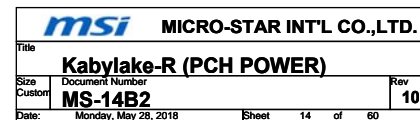
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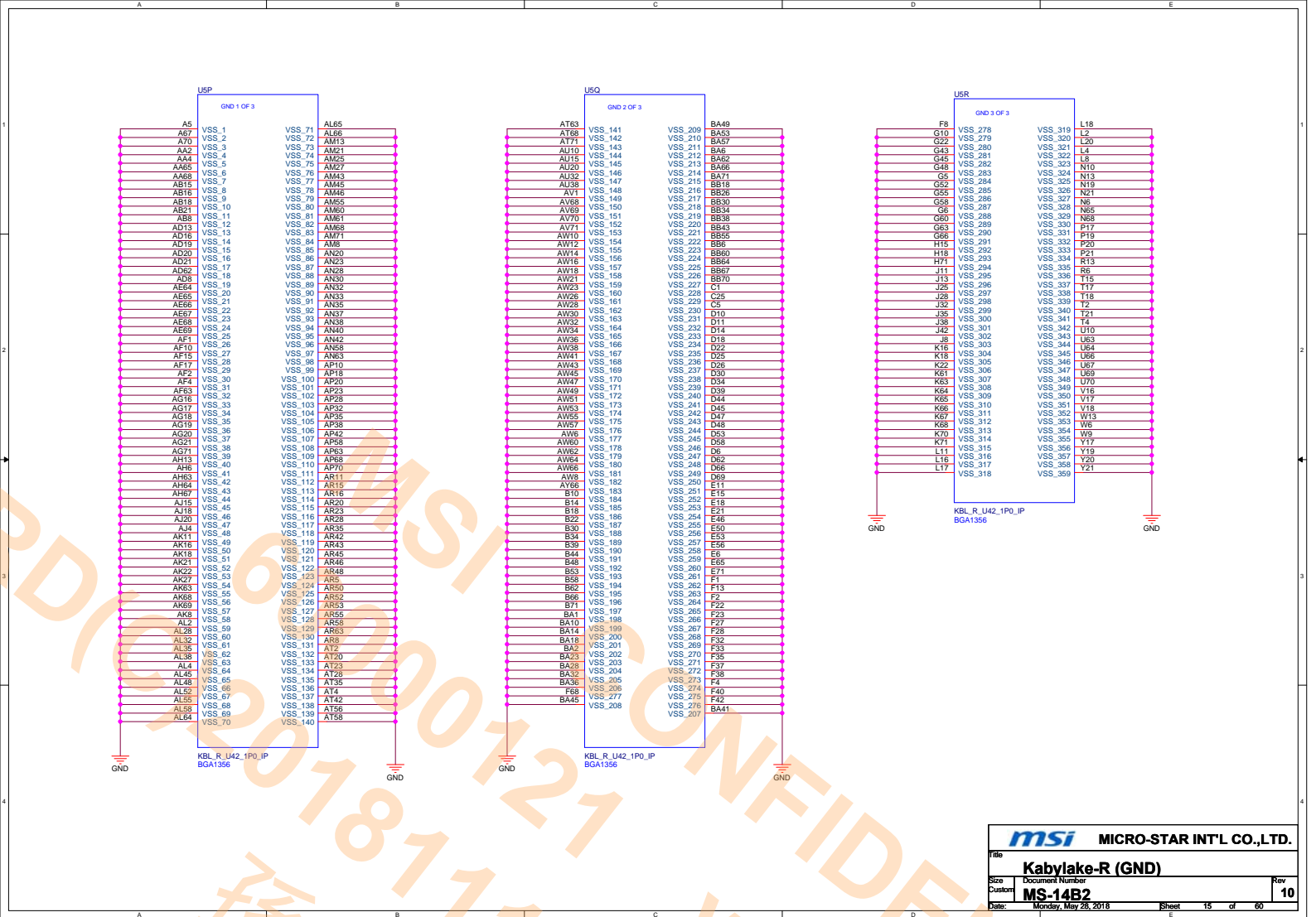
Monday, May 28, 2018

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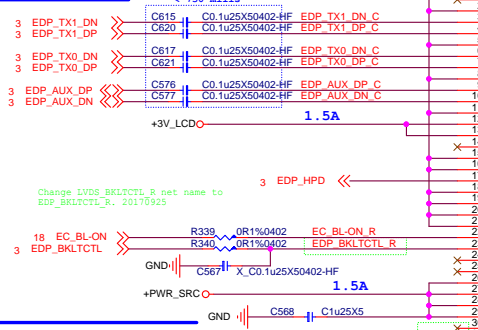






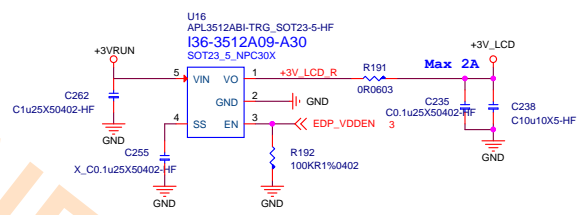
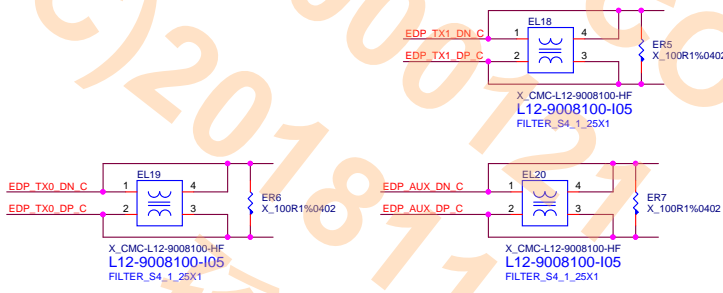
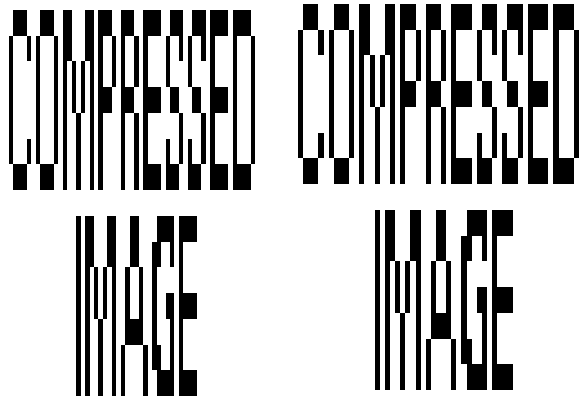
Check cable arrange with ME

eDP



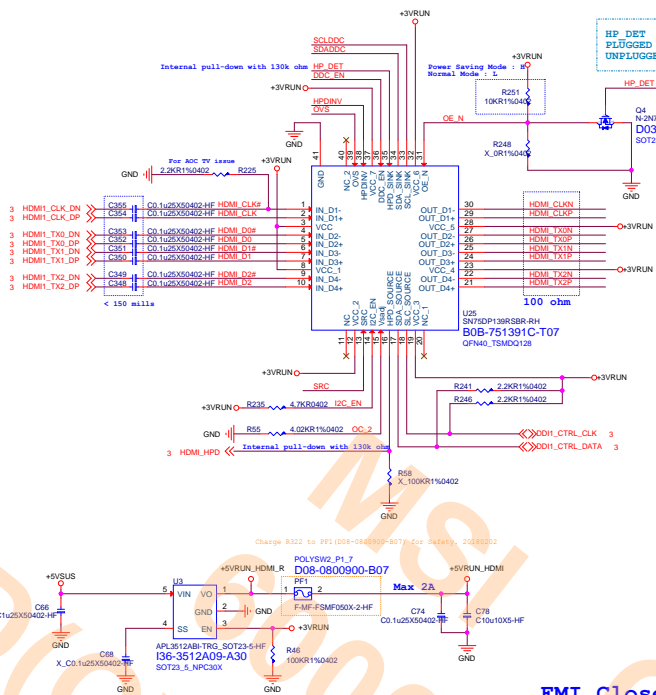
Camera move to Page. 31. 20171116

CON15
FPC40P-0.5PITCH_NATURAL-HF
N5A-40F0180-A81
FPC_S40_10

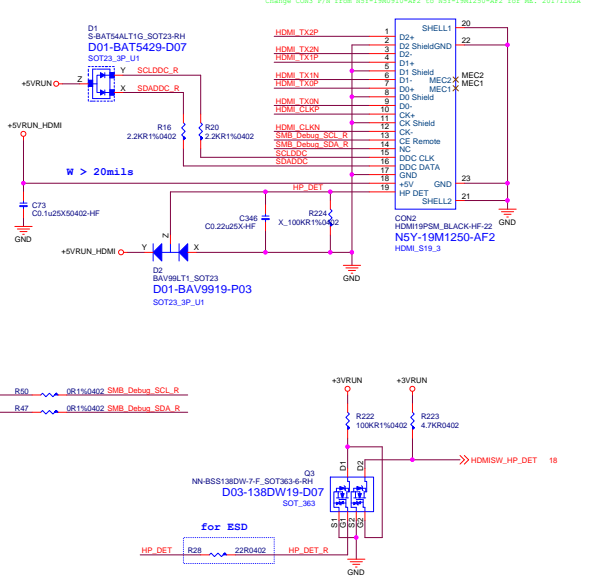


msi MICRO-STAR INT'L CO.,LTD.	
Title eDP Pannel	
Size Custom	Document Number MS-14B2
Date: Monday, May 28, 2018	Rev 10
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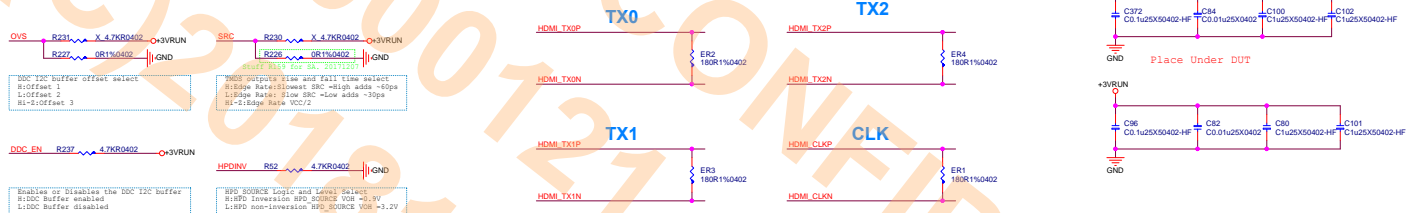
HDMI Level Shifter



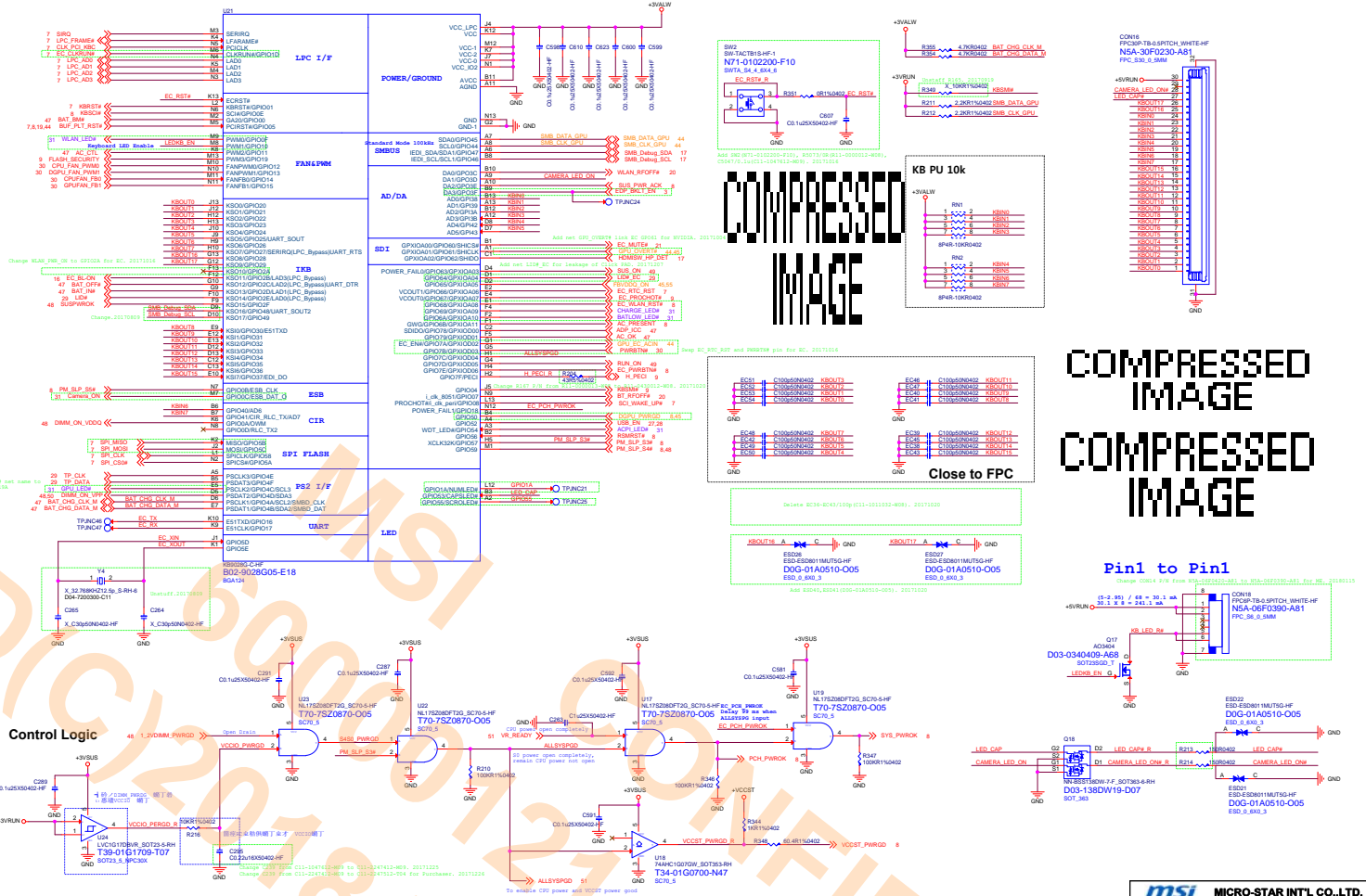
HDMI Connector



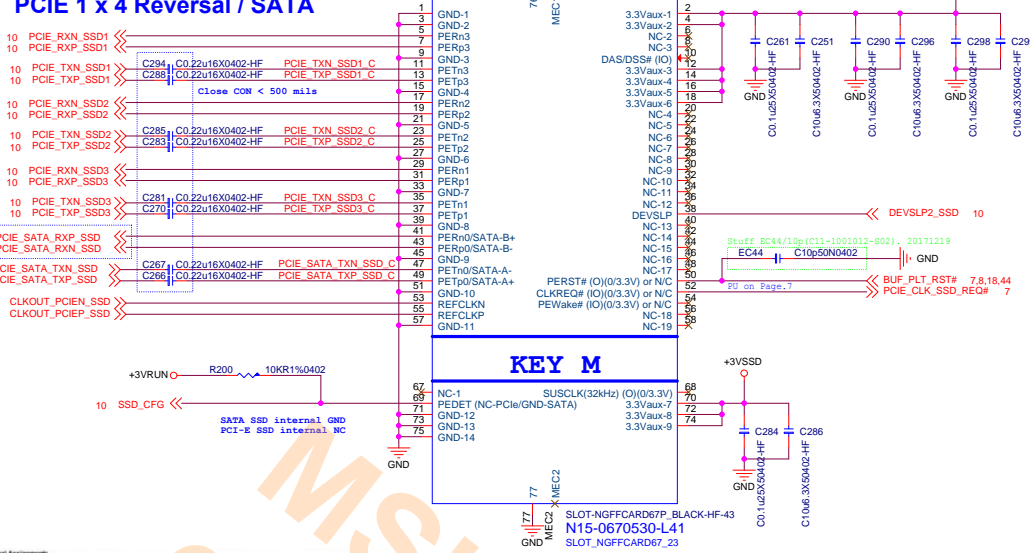
EMI Close Connector



 MICRO-STAR INT'L CO.,LTD.	
Title: HDMI Level Shifter SN75DP139	
Size: Document Number	Rev: 10
Customer: MS-14B2	
Date: Monday, May 28, 2018	Sheet 17 of 60



PCIE 1 x 4 Reversal / SATA



74	3.3V	3.3V	75	3.3V
72	3.3V	3.3V	73	3.3V
70	3.3V	3.3V	71	3.3V
68	3.3V	3.3V	69	3.3V
66	3.3V	3.3V	67	3.3V
64	3.3V	3.3V	65	3.3V
62	3.3V	3.3V	63	3.3V
60	3.3V	3.3V	61	3.3V
58	3.3V	3.3V	59	3.3V
56	3.3V	3.3V	57	3.3V
54	3.3V	3.3V	55	3.3V
52	3.3V	3.3V	53	3.3V
50	3.3V	3.3V	51	3.3V
48	3.3V	3.3V	49	3.3V
46	3.3V	3.3V	47	3.3V
44	3.3V	3.3V	45	3.3V
42	3.3V	3.3V	43	3.3V
40	3.3V	3.3V	41	3.3V
38	3.3V	3.3V	39	3.3V
36	3.3V	3.3V	37	3.3V
34	3.3V	3.3V	35	3.3V
32	3.3V	3.3V	33	3.3V
30	3.3V	3.3V	31	3.3V
28	3.3V	3.3V	29	3.3V
26	3.3V	3.3V	27	3.3V
24	3.3V	3.3V	25	3.3V
22	3.3V	3.3V	23	3.3V
20	3.3V	3.3V	21	3.3V
18	3.3V	3.3V	19	3.3V
16	3.3V	3.3V	17	3.3V
14	3.3V	3.3V	15	3.3V
12	3.3V	3.3V	13	3.3V
10	3.3V	3.3V	11	3.3V
8	3.3V	3.3V	9	3.3V
6	3.3V	3.3V	7	3.3V
4	3.3V	3.3V	5	3.3V
2	3.3V	3.3V	3	3.3V

Pin	Assignment	Description	Pin	Assignment	Description
1	3.3V	3.3V source	1	3.3V	3.3V source
2	3.3V	3.3V source	2	3.3V	3.3V source
3	3.3V	3.3V source	3	3.3V	3.3V source
4	3.3V	3.3V source	4	3.3V	3.3V source
5	3.3V	3.3V source	5	3.3V	3.3V source
6	3.3V	3.3V source	6	3.3V	3.3V source
7	3.3V	3.3V source	7	3.3V	3.3V source
8	3.3V	3.3V source	8	3.3V	3.3V source
9	3.3V	3.3V source	9	3.3V	3.3V source
10	3.3V	3.3V source	10	3.3V	3.3V source
11	3.3V	3.3V source	11	3.3V	3.3V source
12	3.3V	3.3V source	12	3.3V	3.3V source
13	3.3V	3.3V source	13	3.3V	3.3V source
14	3.3V	3.3V source	14	3.3V	3.3V source
15	3.3V	3.3V source	15	3.3V	3.3V source
16	3.3V	3.3V source	16	3.3V	3.3V source
17	3.3V	3.3V source	17	3.3V	3.3V source
18	3.3V	3.3V source	18	3.3V	3.3V source
19	3.3V	3.3V source	19	3.3V	3.3V source
20	3.3V	3.3V source	20	3.3V	3.3V source
21	3.3V	3.3V source	21	3.3V	3.3V source
22	3.3V	3.3V source	22	3.3V	3.3V source
23	3.3V	3.3V source	23	3.3V	3.3V source
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29	3.3V	3.3V source	29	3.3V	3.3V source
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36	3.3V	3.3V source	36	3.3V	3.3V source
37	3.3V	3.3V source	37	3.3V	3.3V source
38	3.3V	3.3V source	38	3.3V	3.3V source
39	3.3V	3.3V source	39	3.3V	3.3V source
40	3.3V	3.3V source	40	3.3V	3.3V source
41	3.3V	3.3V source	41	3.3V	3.3V source
42	3.3V	3.3V source	42	3.3V	3.3V source
43	3.3V	3.3V source	43	3.3V	3.3V source
44	3.3V	3.3V source	44	3.3V	3.3V source
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67	3.3V	3.3V source	67	3.3V	3.3V source
68	3.3V	3.3V source	68	3.3V	3.3V source
69	3.3V	3.3V source	69	3.3V	3.3V source
70	3.3V	3.3V source	70	3.3V	3.3V source
71	3.3V	3.3V source	71	3.3V	3.3V source
72	3.3V	3.3V source	72	3.3V	3.3V source
73	3.3V	3.3V source	73	3.3V	3.3V source
74	3.3V	3.3V source	74	3.3V	3.3V source
75	3.3V	3.3V source	75	3.3V	3.3V source

SSD STAND OFF

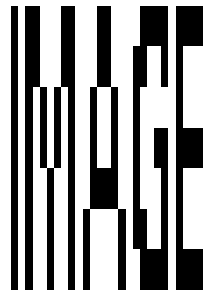
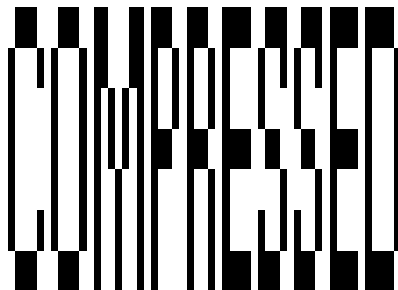
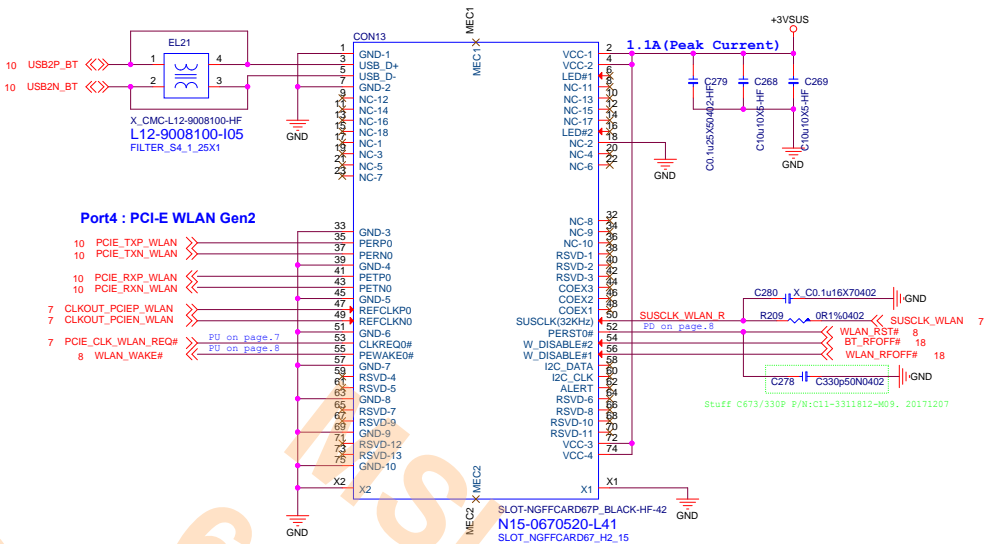
SSD STAND OFF

Spacer UME24
Support E2B-16K1010-RH
H_R201D118_A89
H_R201D118_PT_N

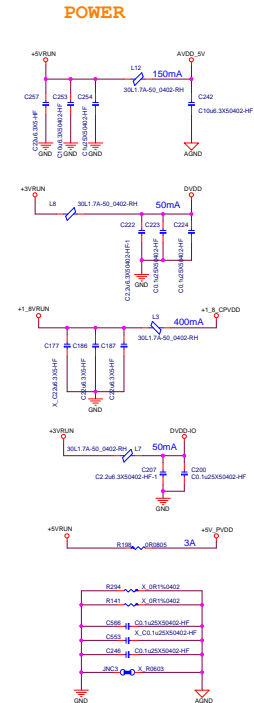
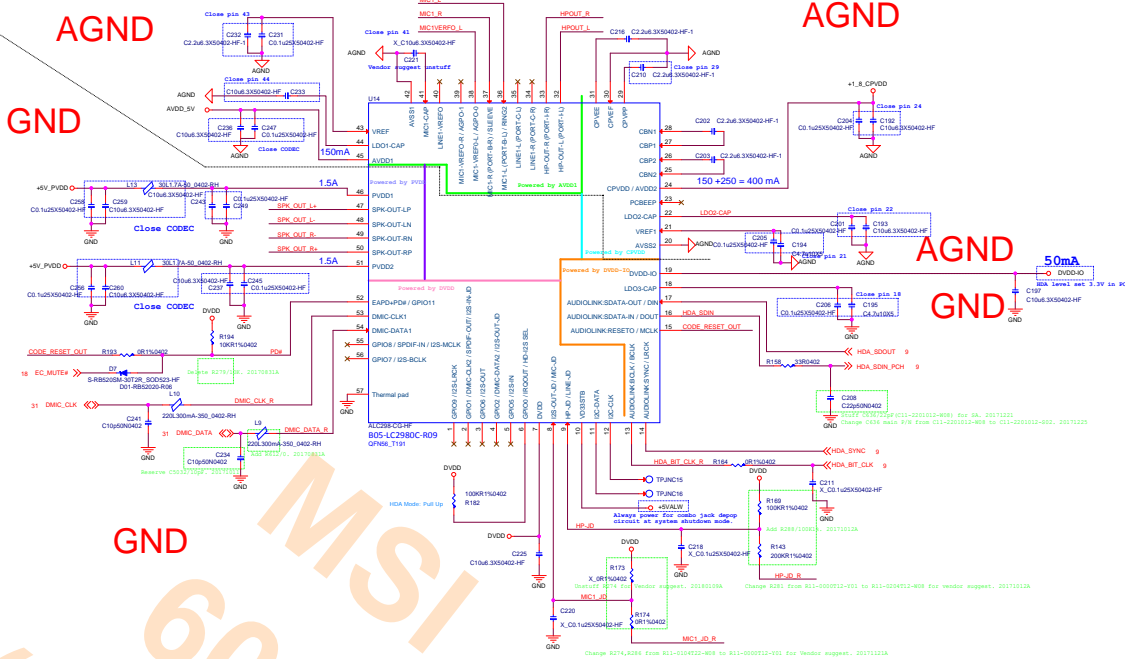
Add UME29 P/N: E2B-16K1010-A89 Footprint: H_R201D118_PT_N for ME. 20171014
Change UME29 Footprint to H_R201D118_PT_N for Layout. 20171030

PCIE	PERp0, PERn0, PETp0, PETn0	IO	PCIE TX/RX Differential signals defined by the PCIe 3.0 specification
	PERp1, PERn1, PETp1, PETn1		
	PERp2, PERn2, PETp2, PETn2		
	PERp3, PERn3, PETp3, PETn3		
	REFCLK+ REFCLK-	I	PCIE Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification
	PERST#	O	PE-Reset is a functional reset to the card as defined by the PCIe Mini Card CEM specification
	CLKREQ#	IO	Clock Request is a reference clock request signal as defined by the PCIe Mini Card CEM specification; Also used by L1 PM Substates
	WAKE#/OBFF	IO	PCIE PME Wake. Open Drain with pull up on platform; Active Low

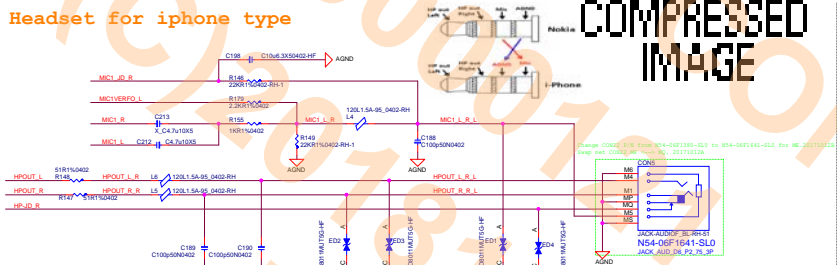
msi MICRO-STAR INT'L CO., LTD.	
Title M.2 KEY-M Combo SSD	
Size	Document Number MS-14B2
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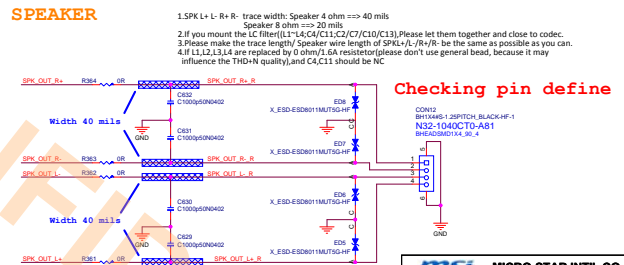
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Title	M.2 KEY-E WLAM(9260)
Size	Document Number
Custom	MS-14B2
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Headset for iphone type



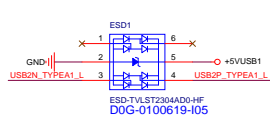
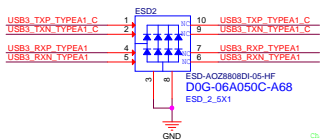
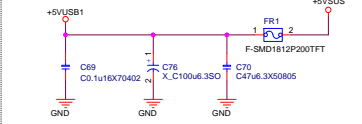
SPEAKER



MSI 60000121 CONFIDENTIAL
PD(C)2018111520001 weilu(盧偉)
孫飛(60010839) 客戶服務部

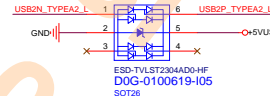
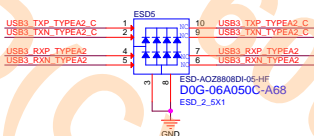
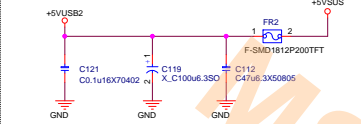
msi MICRO-STAR INT'L CO.,LTD.	
U3 Re-driver TYPE-A Port1.2	
Size	Document Number
Conf	MS-14B2
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USB Power Switch

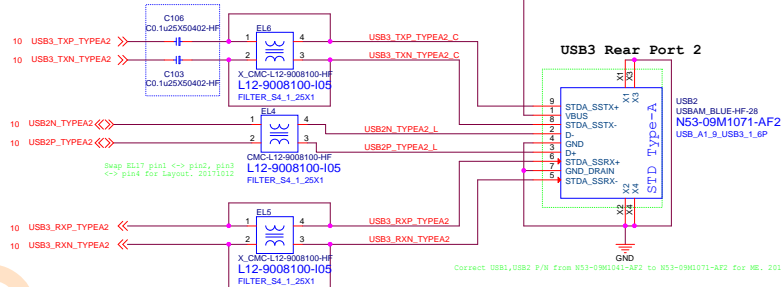


Change USB2N_TYPEA1_L, USB2P_TYPEA1_L from R2023.1, R2023.6 to R2023.3, R2023.4 for Layout. 20180119

USB Power Switch



Close to Connector



Swap EL17 pin1 <-> pin2, pin3 <-> pin4 for Layout. 20171012

Correct USB1,USB2 P/N from N53-09M1071-AF2 to N53-09M1071-AF2 for ME. 201710128

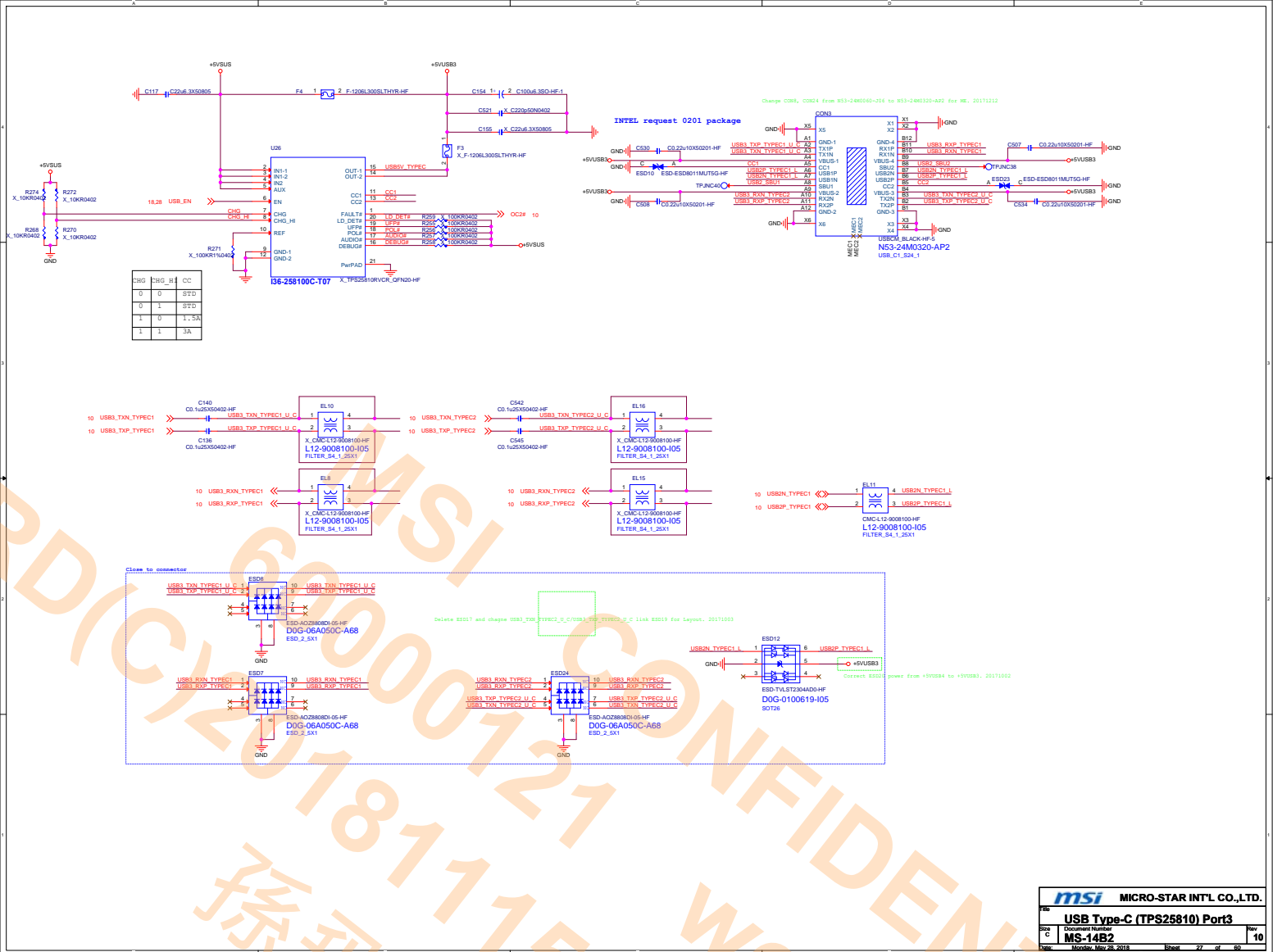
msi MICRO-STAR INT'L CO.,LTD.			
Title			
USB3 Type-A Port1.2			
Size			
Customer			
MS-14B2			
Date			
Version			
Rev			
10			

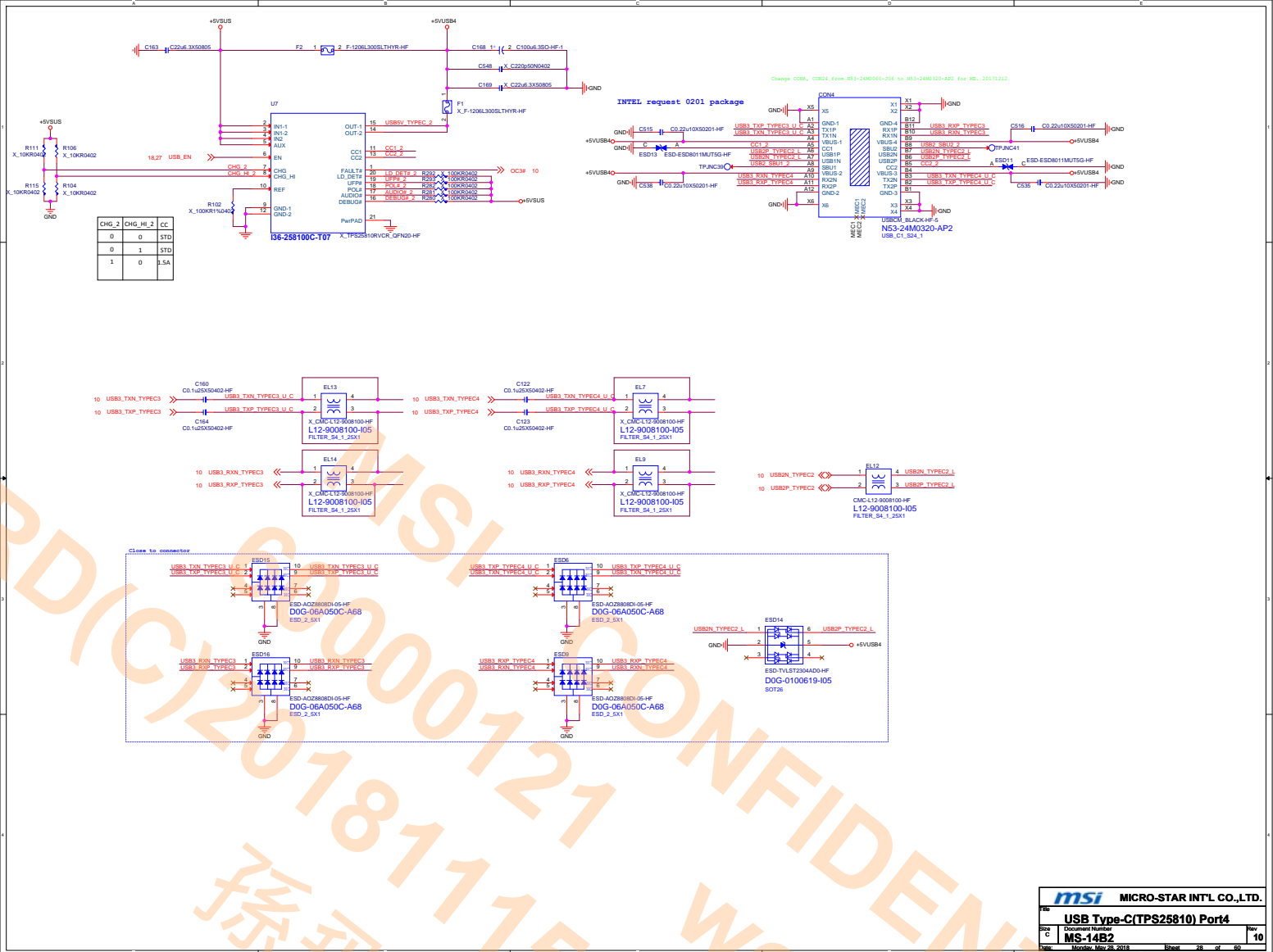
MSI 60000121 CONFIDENTIAL
weilu(盧偉)
客戶服務部
孫飛(60010839)
PD(C)2018111520001

msi		MICRO-STAR INT'L CO.,LTD.	
Title		U3 Re-driver TYPE-C Port3	
Size	Document Number	Rev	
Conf	MS-14B2	10	
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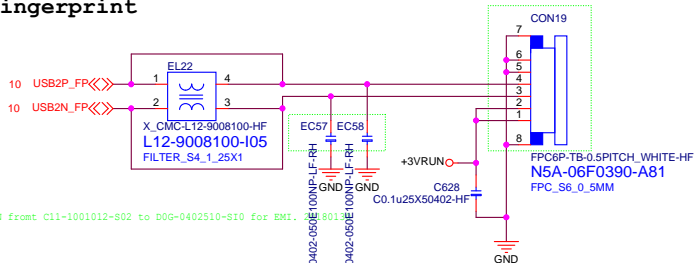
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msi		MICRO-STAR INT'L CO.,LTD.	
Title		U3 Re-driver TYPE-C Port4	
Size	Document Number	Rev	
Config	MS-14B2	10	
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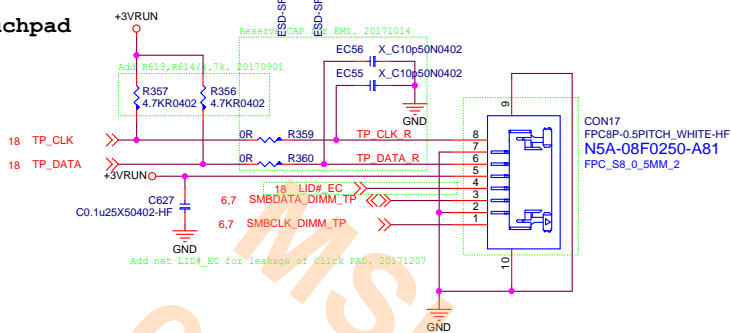


Fingerprint



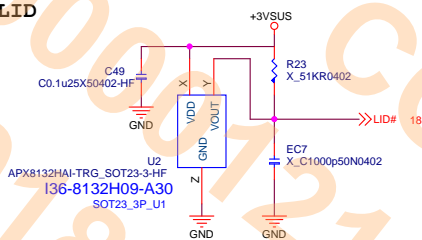
COMPRESSED
IMAGE

Touchpad



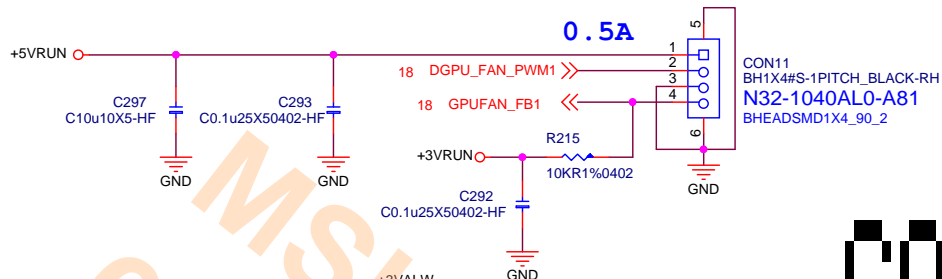
COMPRESSED
IMAGE

LID




msi MICRO-STAR INT'L CO.,LTD.			
Title Click,FingerPrint,LID			
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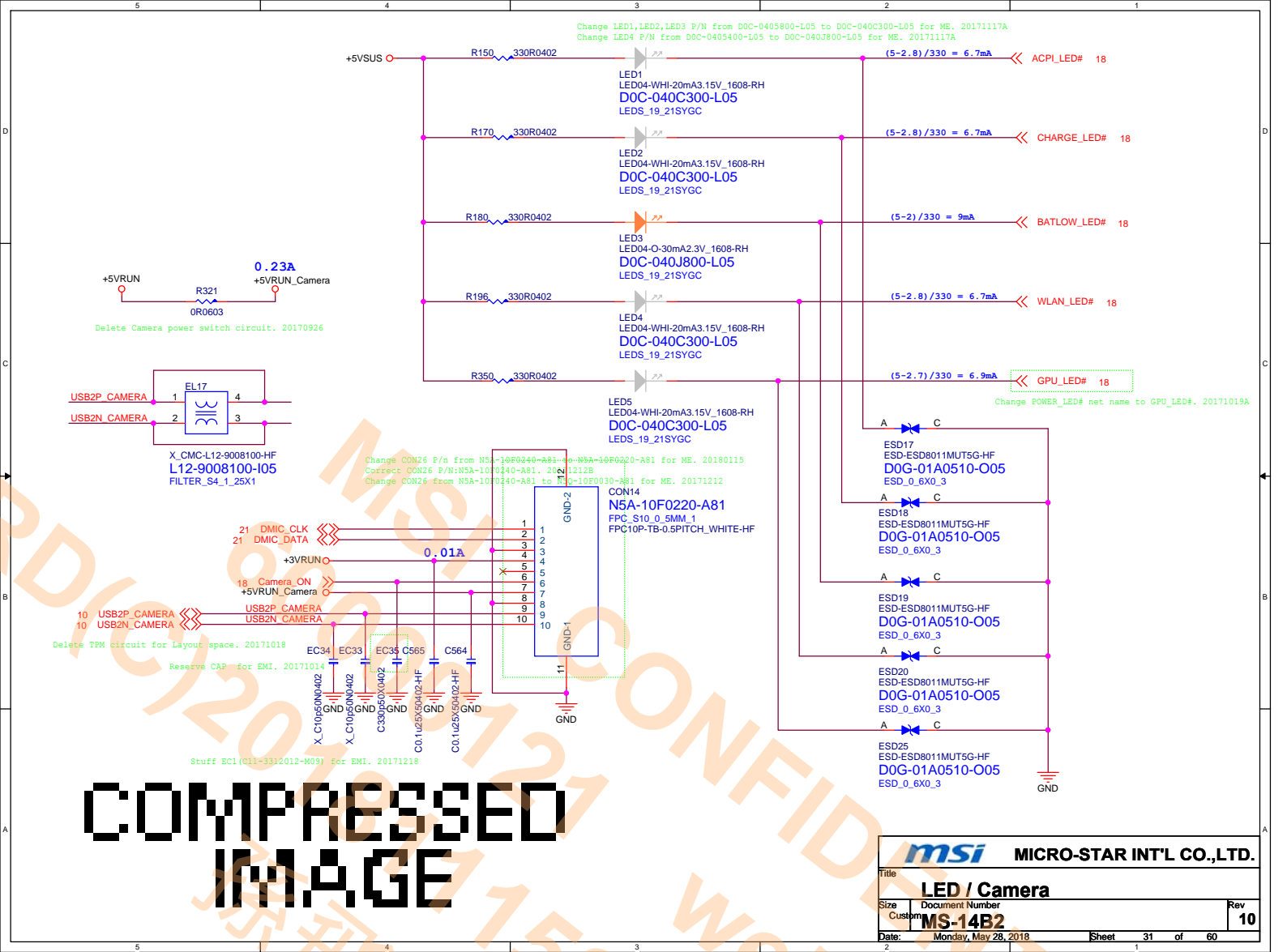
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IMAGE



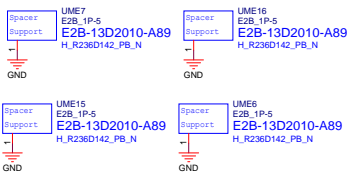
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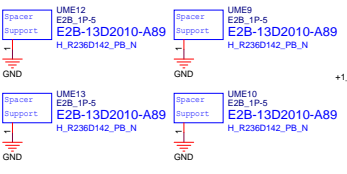
 MICRO-STAR INT'L CO.,LTD.	
Title	
FAN,Power SW	
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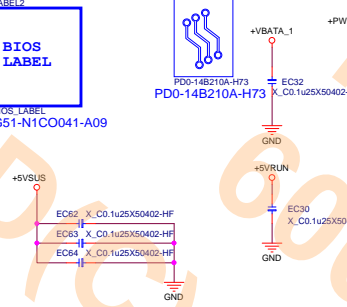
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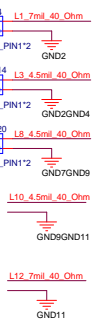
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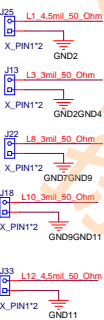
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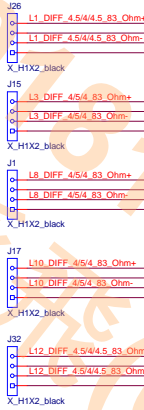
Single 40 Ohm



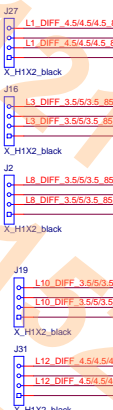
Single 50 Ohm



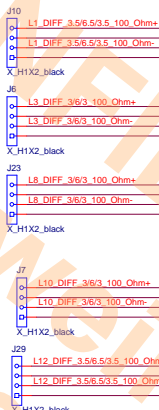
Differential 83 Ohm



Differential 85 Ohm



Differential 100 Ohm



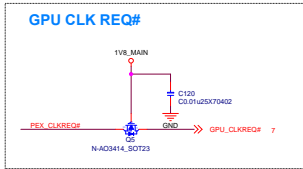
6

4

3

2

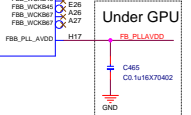
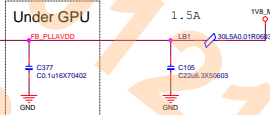
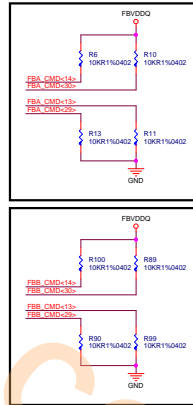
msi MICRO-STAR INT'L CO., LTD.	
Title	ME,EMI
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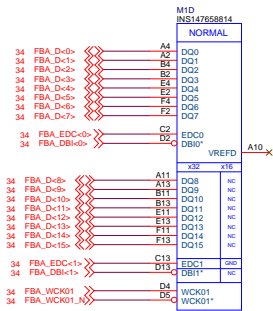
GPU Frame Buffer Partition A/B

GDD5 Command Mapping GB4C-128

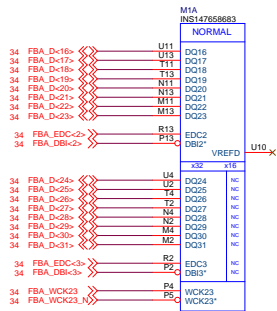
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3 BA3
CMD2	CMD18	A2 BA0
CMD3	CMD19	A4 BA2
CMD4	CMD20	A5 BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7 A8
CMD7	CMD23	A6 A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12 RFU
CMD10	CMD26	A0 A10
CMD11	CMD27	A1 A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CAS*
CMD15	CMD31	CAS*



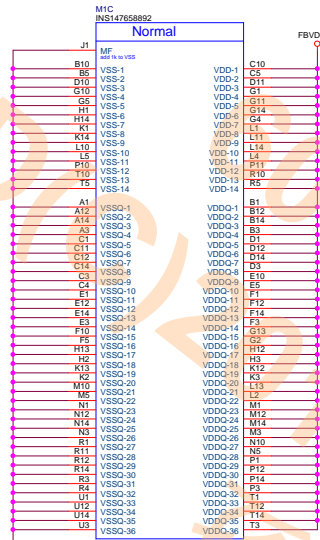
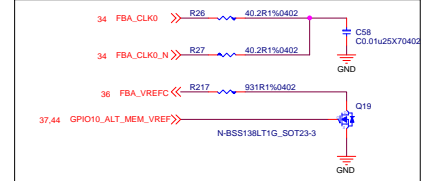
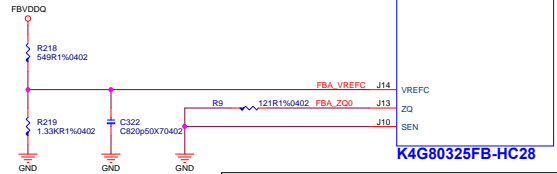
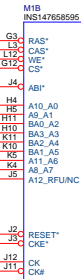
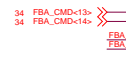
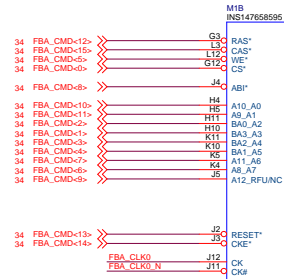
DGPU_GDDR5 FrameBuffer A0



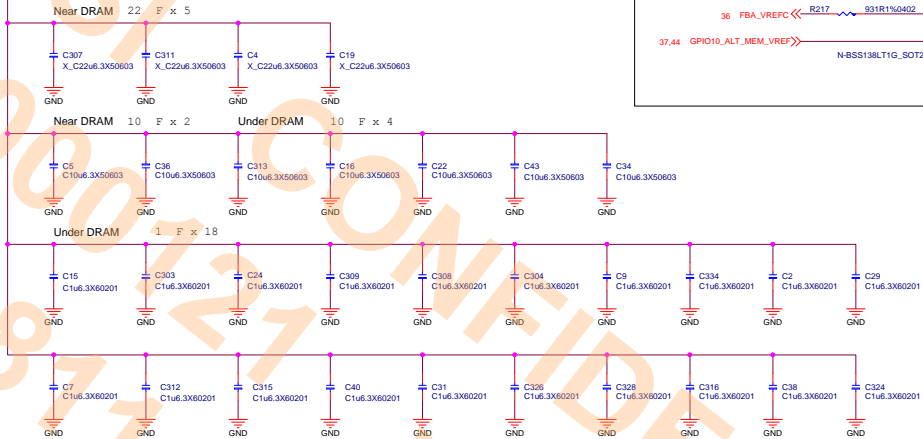
K4G80325FB-HC28




K4G80325FB-HC28

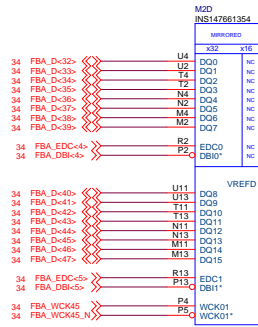


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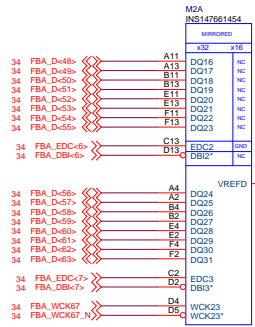


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DGPU GDDR5 FrameBuffer A0			
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DGPU_GDDR5 FrameBuffer A1

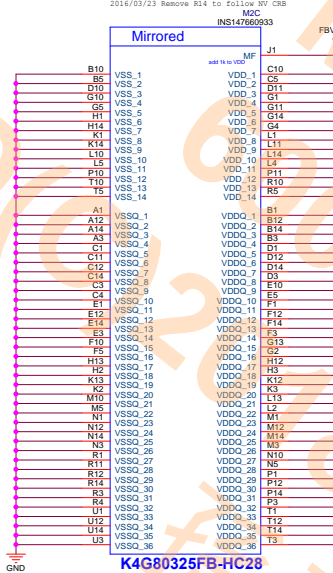
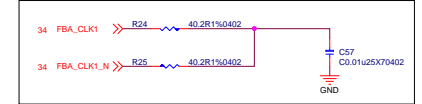
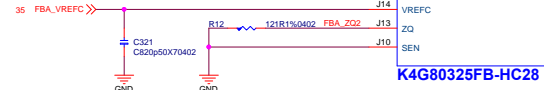
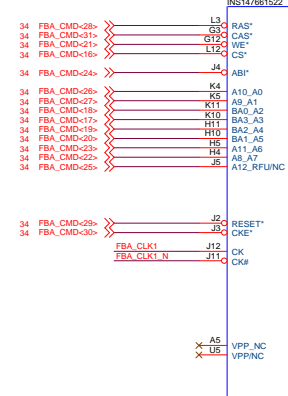


K4G80325FB-HC28

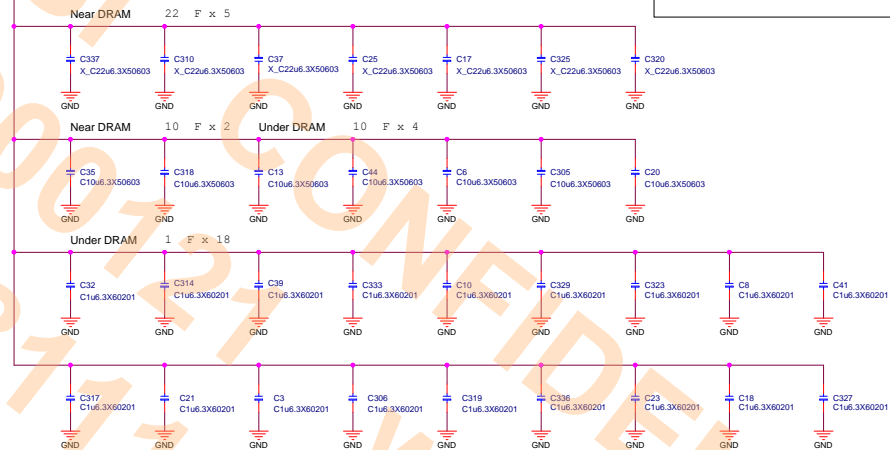


K4G80325FB-HC28

M12-8032545-S02

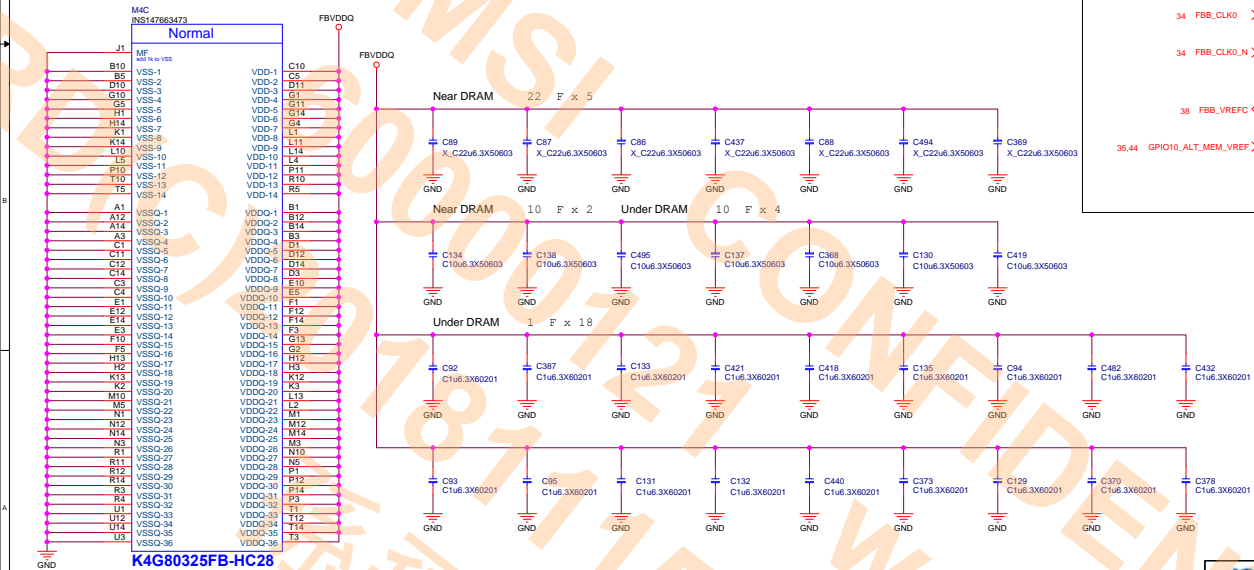
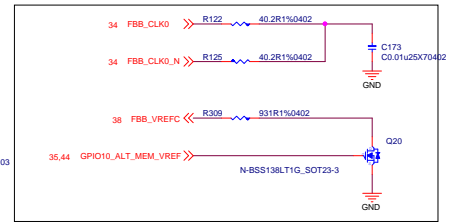
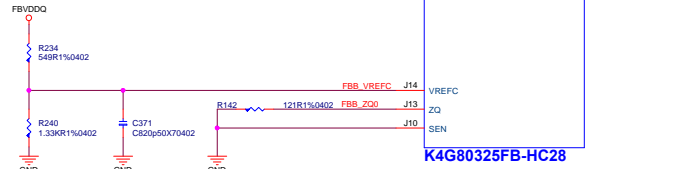
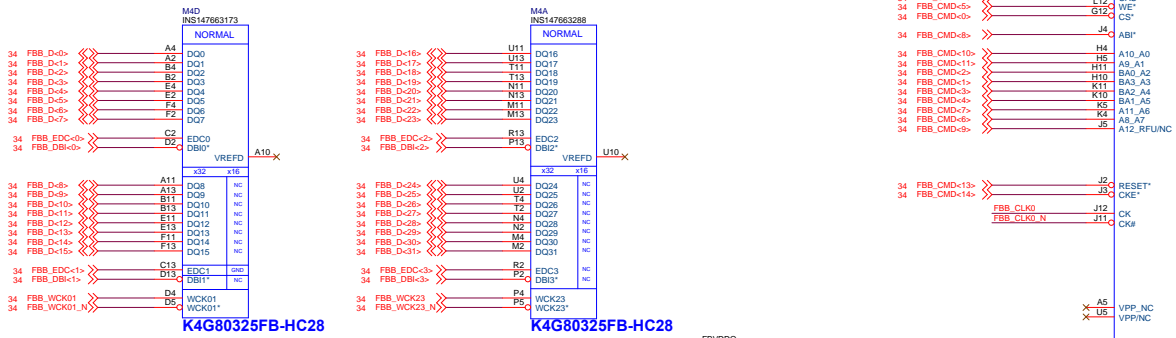


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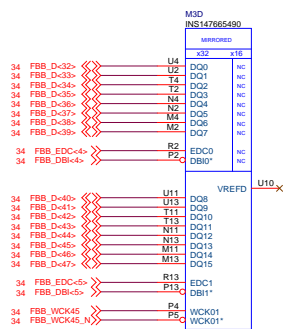


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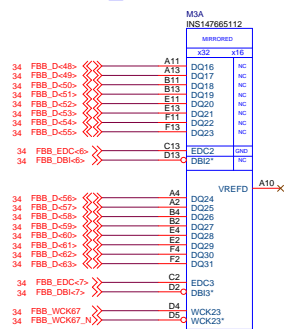
DGPU_GDDR5 FrameBuffer B0



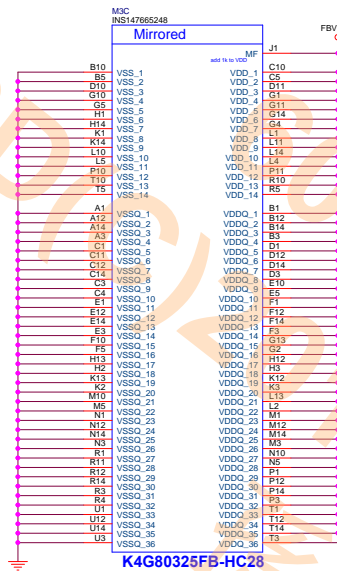
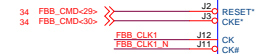
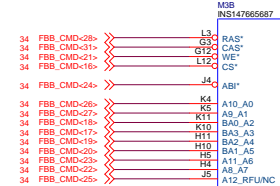
DGPU_GDDR5 FrameBuffer B1



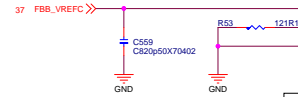
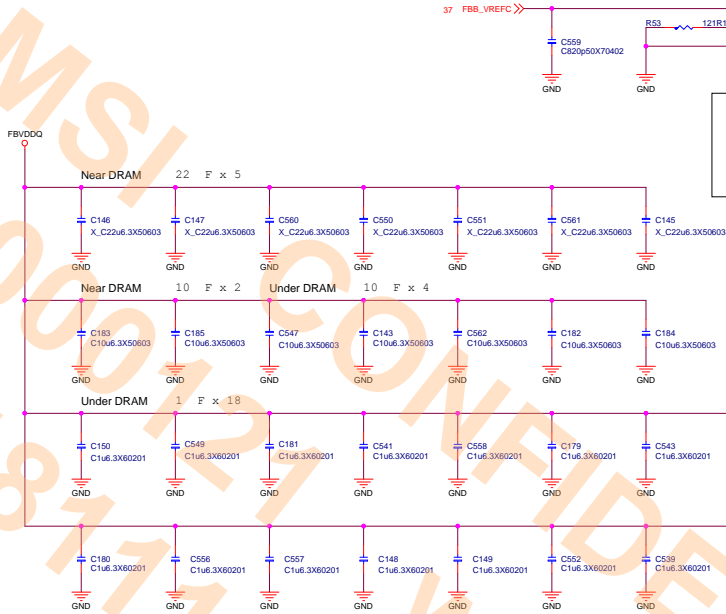
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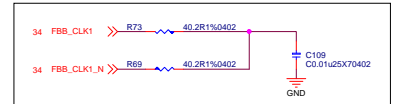
K4G80325FB-HC28



K4G80325FB-HC28



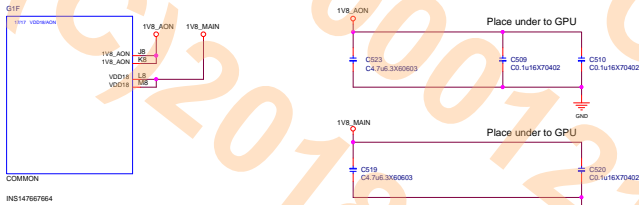
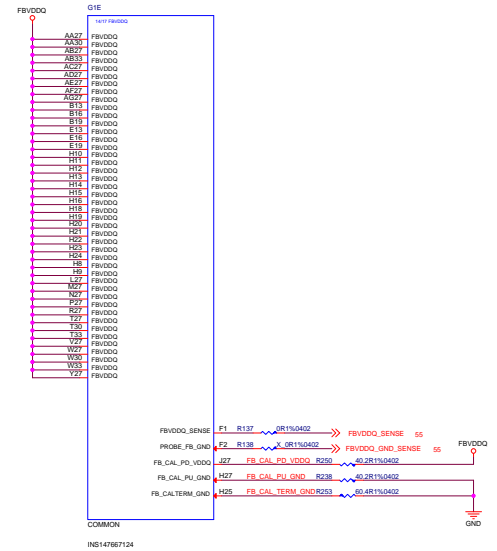
K4G80325FB-HC28




The schematic diagram illustrates the power and sense connections for the DGPU section. Key components and connections include:

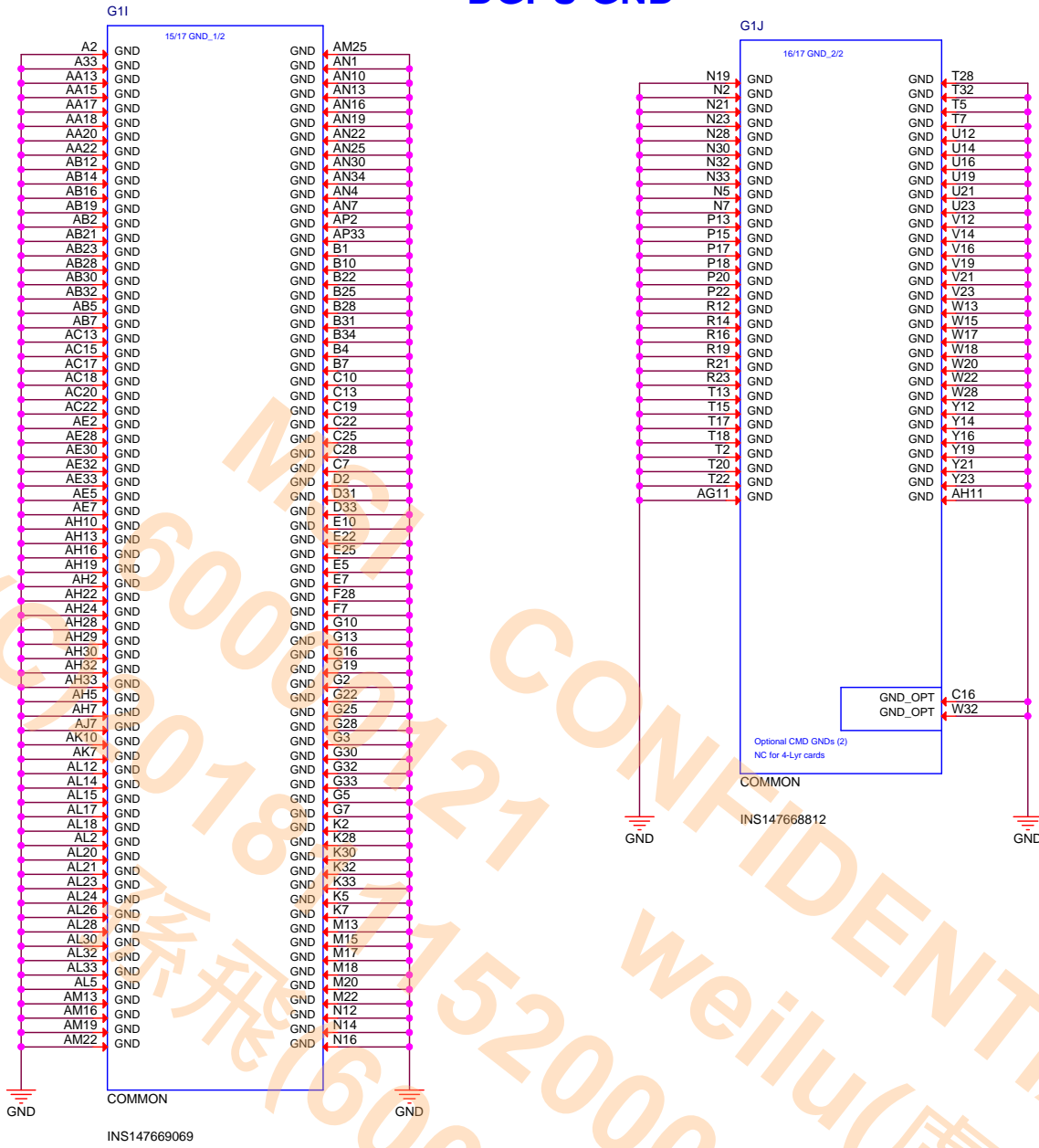
- Power and Sense Lines:** VDD_SENSE, GND_SENSE, NVVDD_SENSE_GPU, and NVVDD_GND_SENSE_GPU are shown with their respective connections to the GPU and the system.
- Capacitors:** C503, C509, C510, C519, and C520 are connected to the power lines, with values ranging from 100nF to 1000nF.
- Resistors:** R307 and R303 are connected to the sense lines, with values of 100R and 100R respectively.
- Table:** A table at the bottom right provides document information, including the document number MS-14B2 and the date of revision.


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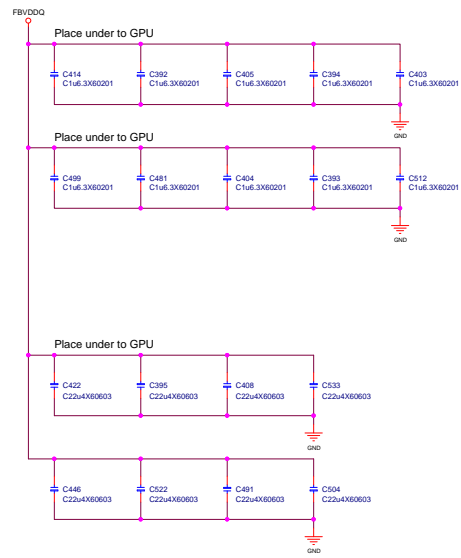
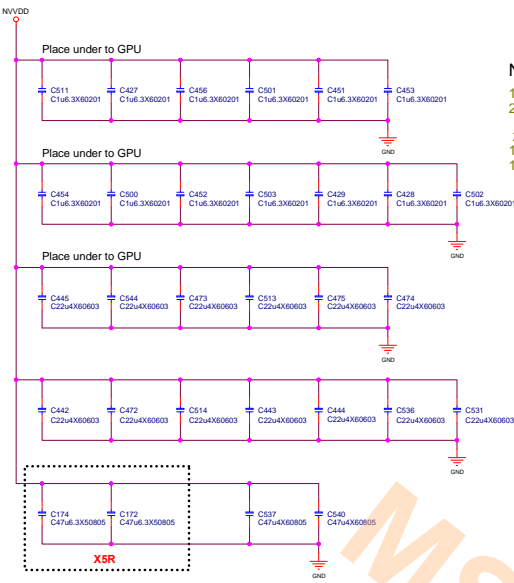
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DGPU POWER			
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DGPU GND



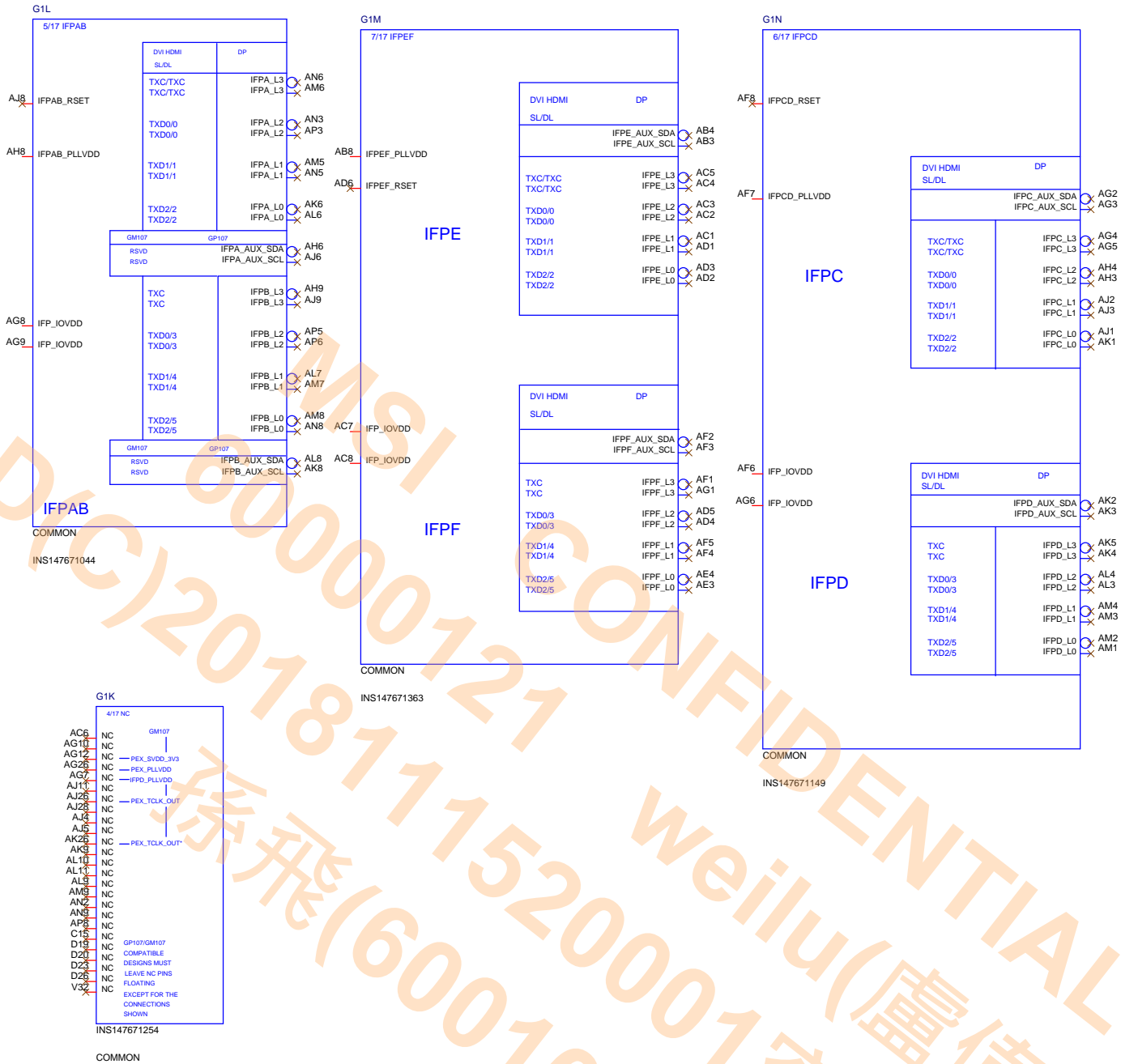
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DGPU GND			
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GPU DECOUPLING

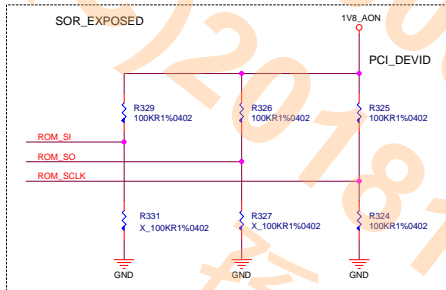
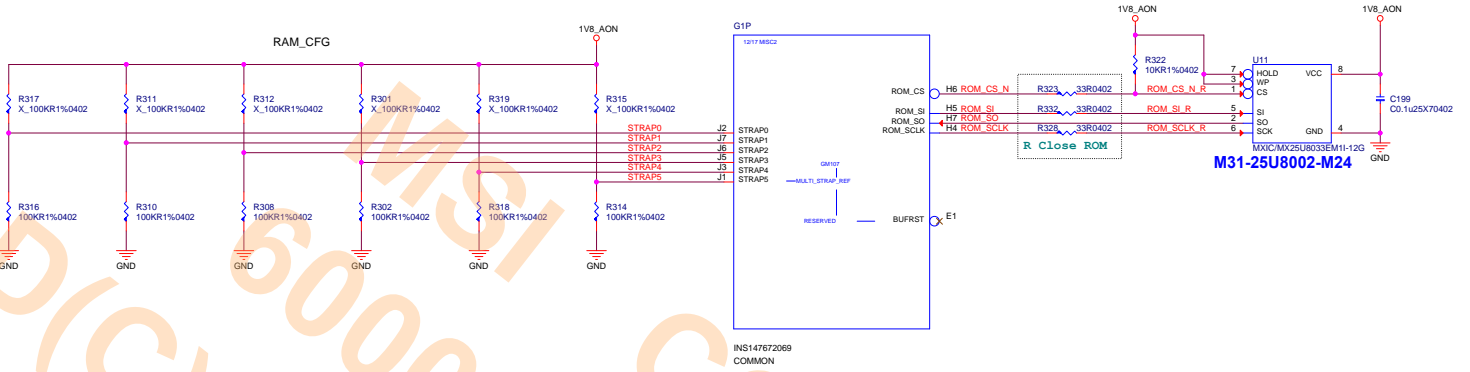
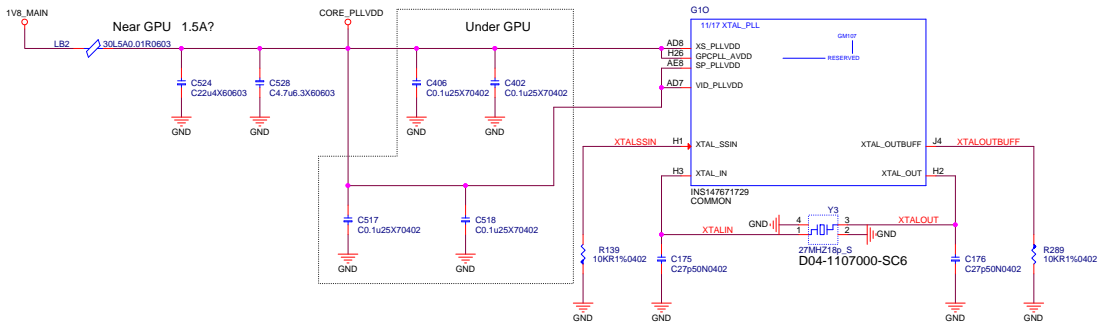


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DACA,Display IF



ROM, MULTI-LEVEL STRAPS

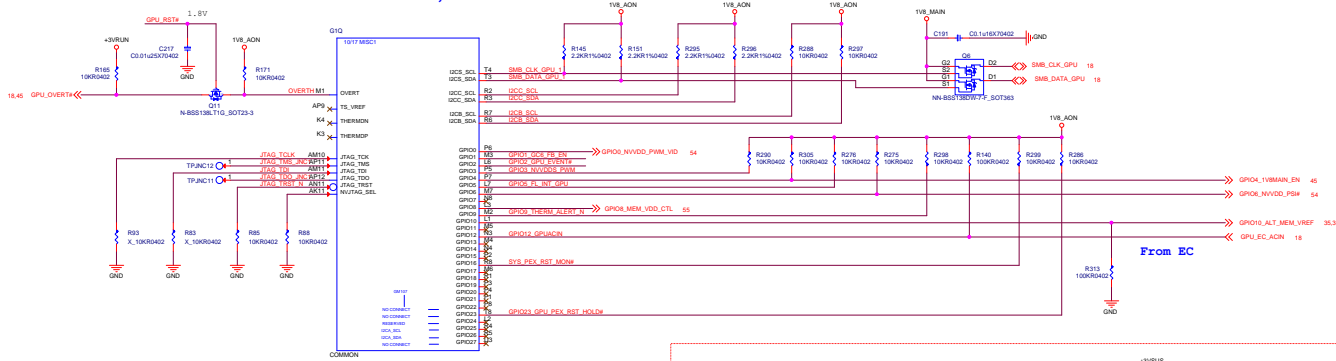


STRAP 5	STRAP 4	STRAP 3	
L	L	L	Optimus
L	L	H	Discrete
H	L	H	Discrete with Gsync

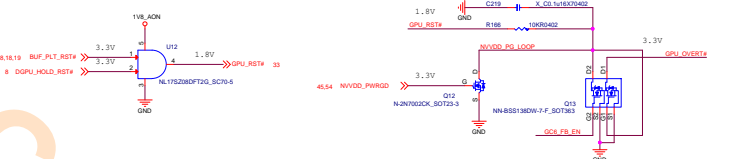
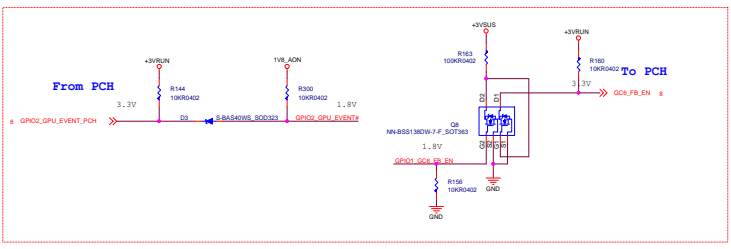
STRAP 2	STRAP 1	STRAP 0			
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L	L	L	0x0	Samsung K4G80325FB-BC28	
L	L	H	0x1	Microm MT51J2256M32HF-80-A	
L	H	L	0x2	Hynix H5G6C8H24MJR-R4C	128M*32
H	H	L	0x6	Hynix H5GQ4H24AJR-R4C	
H	H	H	0x7	Samsung K4G41325FE-BC25	

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED3	SOR_EXPOSED2	SOR_EXPOSED1	SOR_EXPOSED0
L	L	L	1:ENABLE	1:ENABLE	1:ENABLE	1:ENABLE
L	L	H	1:ENABLE	1:ENABLE	1:ENABLE	0:DISABLE
L	H	L	1:ENABLE	1:ENABLE	0:DISABLE	1:ENABLE
L	H	H	1:ENABLE	1:ENABLE	0:DISABLE	0:DISABLE
H	H	H	1:ENABLE	0:DISABLE	0:DISABLE	0:DISABLE
H	H	M	0:DISABLE	0:DISABLE	0:DISABLE	0:DISABLE

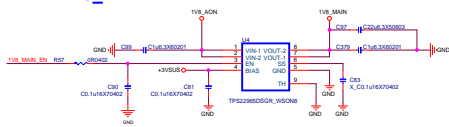
DGPU GPIO, I2C



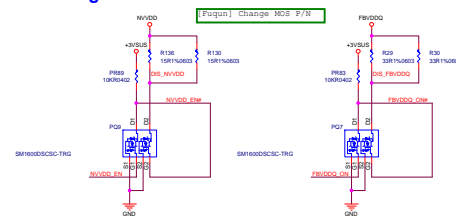
Pin Name	Normal function	I/O	Functional Description	Recommended Default
GPIO0	NVVDOS_PFM	O	PFM Output to control NVVDOS	Pull-up or pull-down
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	0Ω, 10K pull-up to V8_AON
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to V8_AON
GPIO3	NVVDOS_PFM	O	PFM output to control the NVVDOS power supply	0 to V8 output
GPIO4	V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	0Ω, 10K pull-up to V8_AON
GPIO5	PFM_LCK#	I	Active low Frame Lock	0Ω, 10K pull-up to V8_AON
GPIO6	NVVDOS_PFM	O	PFM output to control the NVVDOS power supply	10K pull-up to V8_AON
GPIO7	LCD_BL_PFM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	100K pull-down
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	0Ω, 10K pull-up to V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PFM_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	RFD_A	I	Rot Plug Detect for IFPA	10K pull-up to V8_AON
GPIO15	RFD_B	I	Rot Plug Detect for IFPB	10K pull-up to V8_AON
GPIO16	SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10K pull-up to V8_AON
GPIO17	RFD_D	I	Rot Plug Detect for IFPD	10K pull-up to V8_AON
GPIO18	RFD_E	I	Rot Plug Detect for IFPE	10K pull-up to V8_AON
GPIO19	3D Vision	O	3D Vision L/R signal	100K pull-down
GPIO20	GC6_FB_EN	O	GC6 FB Enable	0Ω, 10K pull-up to V8_AON
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		
GPIO23	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	0Ω, 10K pull-up to 4 pinled v93
GPIO24	RFD_F	I	Rot Plug Detect for IFPF	10K pull-up to V8_AON
GPIO25	UNUSED	I/O		
GPIO26	UNUSED	I/O		
GPIO27	RFD_C	I	Rot Plug Detect for IFPC	10K pull-up to V8_AON



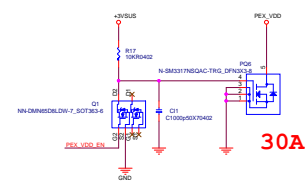
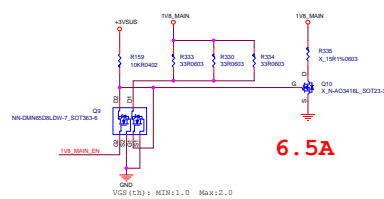
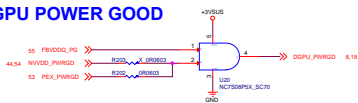
1V8_MAIN



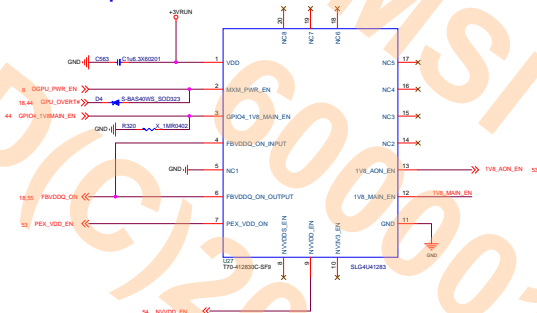
Discharge



DGPU POWER GOOD



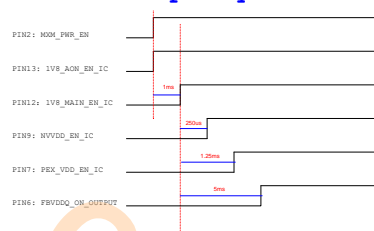
Power Sequence Control



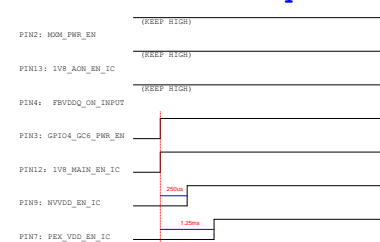
PIN2: MXM PWR_EN is 3.3V
 PIN3: GPIO4_GC6_PWR_EN is 1.8V
 PIN4: FBVDDQ_ON INPUT 3.3V
 PIN6: FBVDDQ_ON OUTPUT 3.3V
 PIN7: PEX_VDD_EN IC 3.3V
 PIN9: NVVDD_EN IC 3.3V
 PIN12: 1V8_MAIN_EN IC 3.3V
 PIN13: 1V8_AON_EN IC 3.3V

INPUT
 INPUT
 INPUT
 OUTPUT
 OUTPUT
 OUTPUT
 OUTPUT

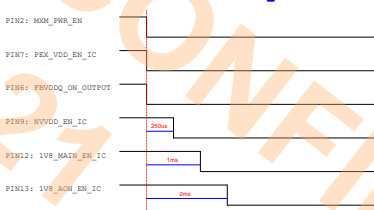
Power Up Sequence



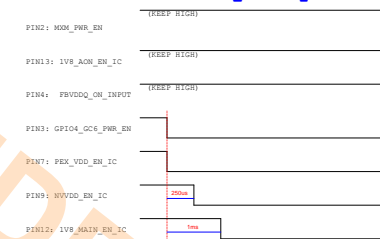
GC6 2.1 Exit Sequence



Power Down Sequence

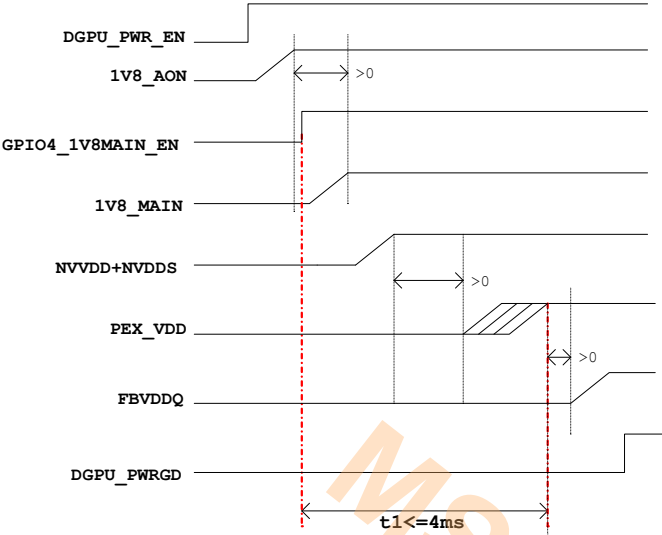


GC6 2.1 Entry Sequence



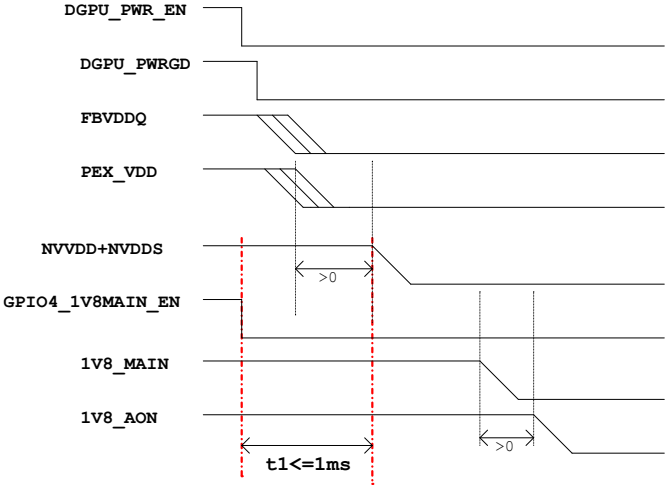
POWER UP Sequence

1V8_AON -> 1V8_MAIN->NV3V3 -> NVVDD -> NVVDDS / PEX_VDD -> FBVDDQ

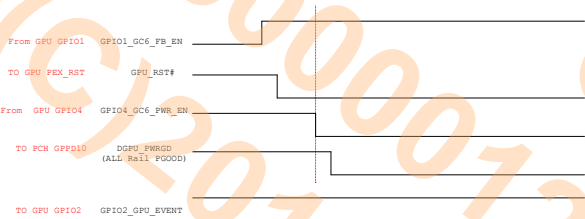


POWER Down Sequence

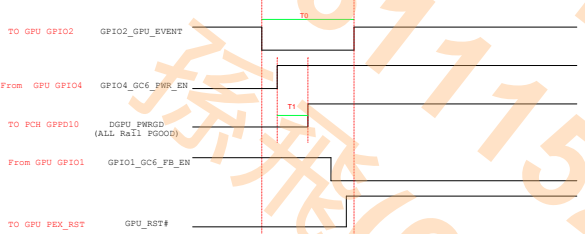
NVVDDS/PEX_VDD/FBVDDQ ->NVVDD/NV3V3->1V8_MAIN> 1V8_AON



GC6 2.1 ENTRY SEQUENCE



GC6 2.1 EXIT SEQUENCE



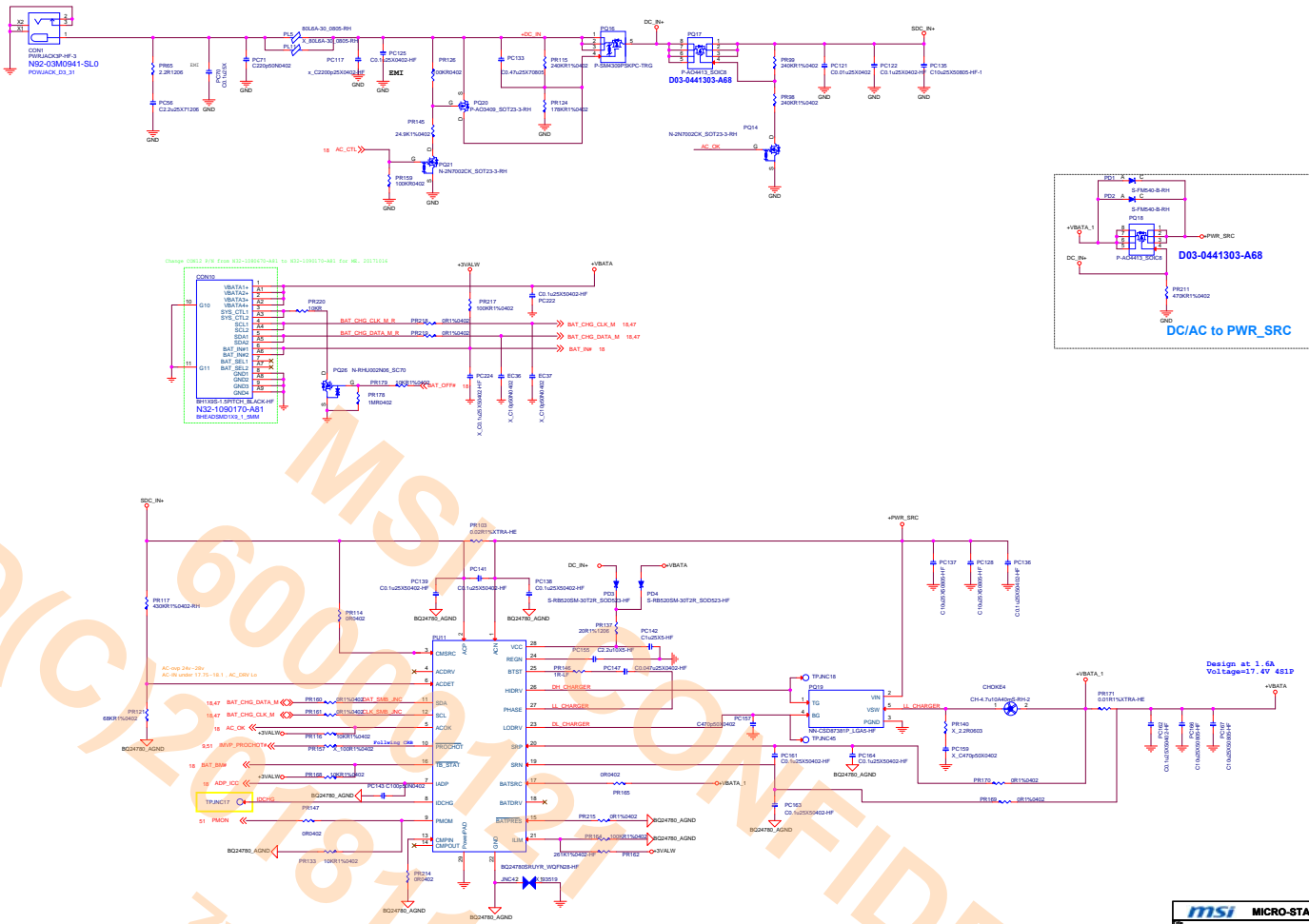
GC6 2.1 TIMING

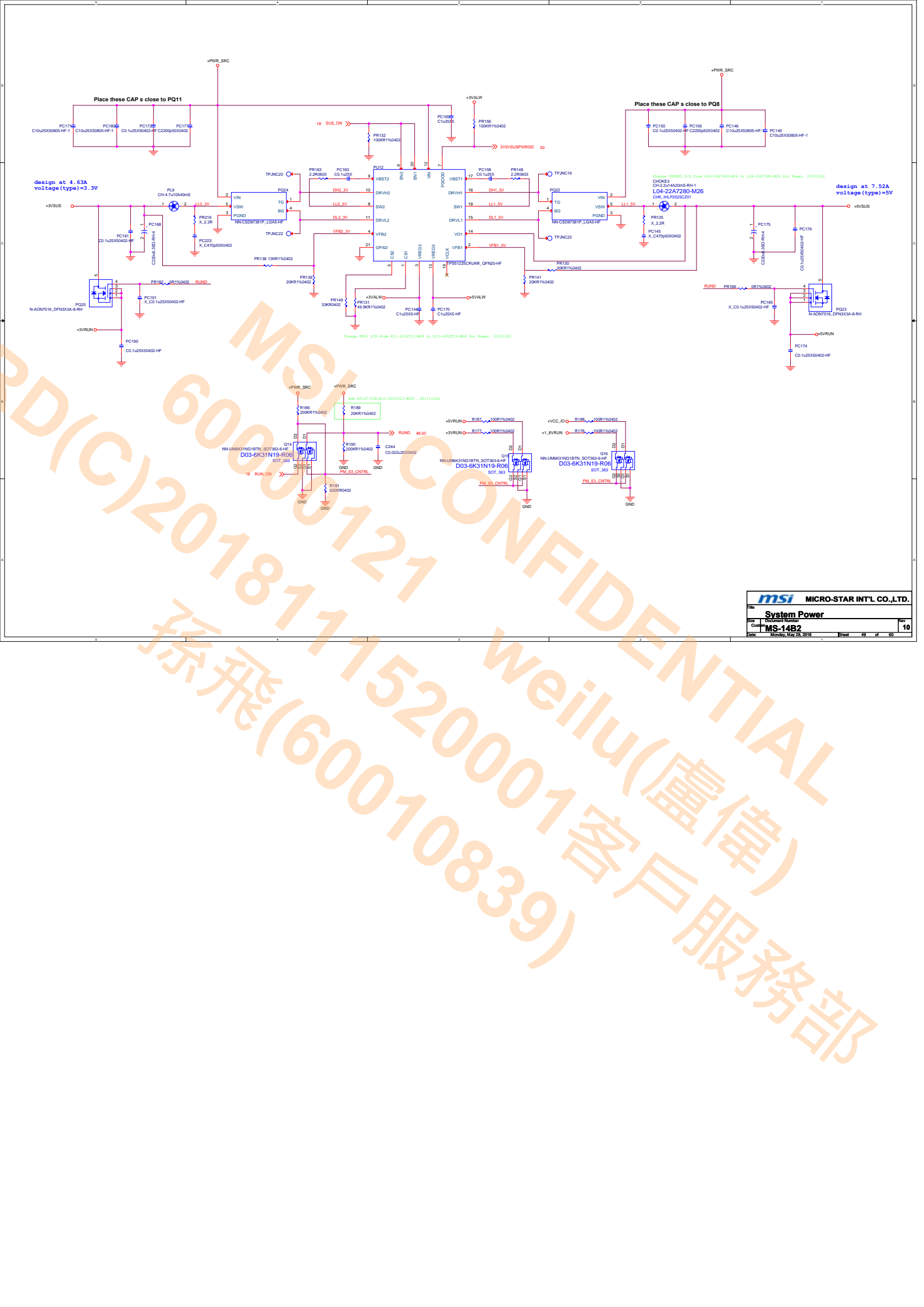
	Min	Max	Unit	Description
T0	0.001	N/A	ms	GPU_EVENT# assertion
T1	0.04	4	ms	3V3_MAIN_EN assertion to all power rails up and stable

NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot ge guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

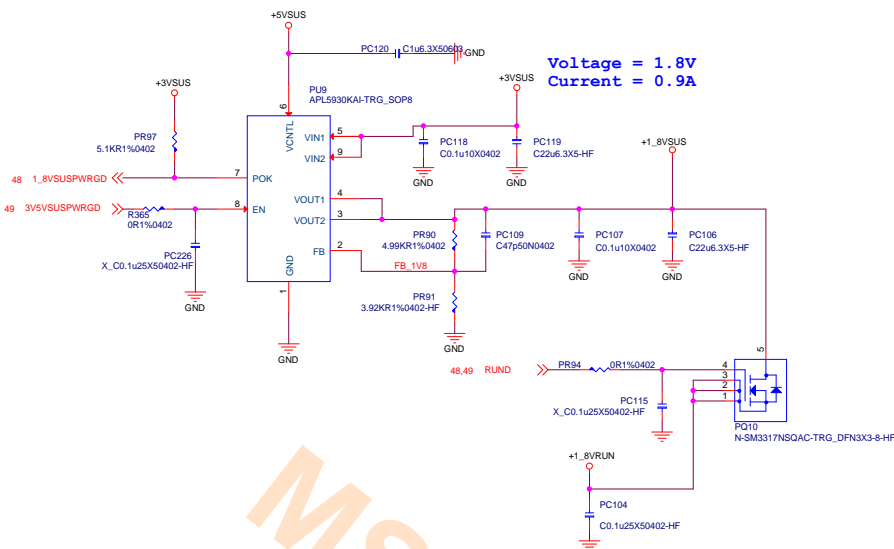
Adapter = 65w
Adapter voltage = 19v



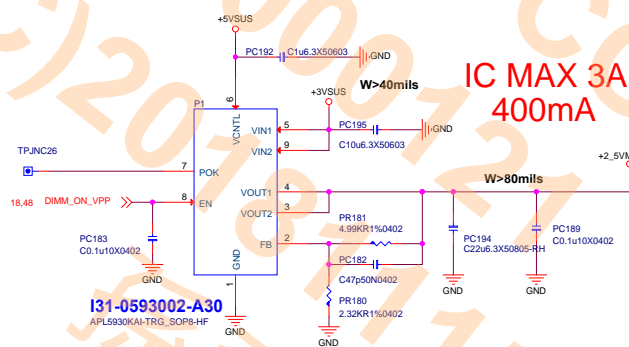


msi MICRO-STAR INT'L CO.,LTD.			
File	System Power		
Size	Record Number		
MS-14B2			
Date	Monday, May 28, 2018	Board	48 of 50

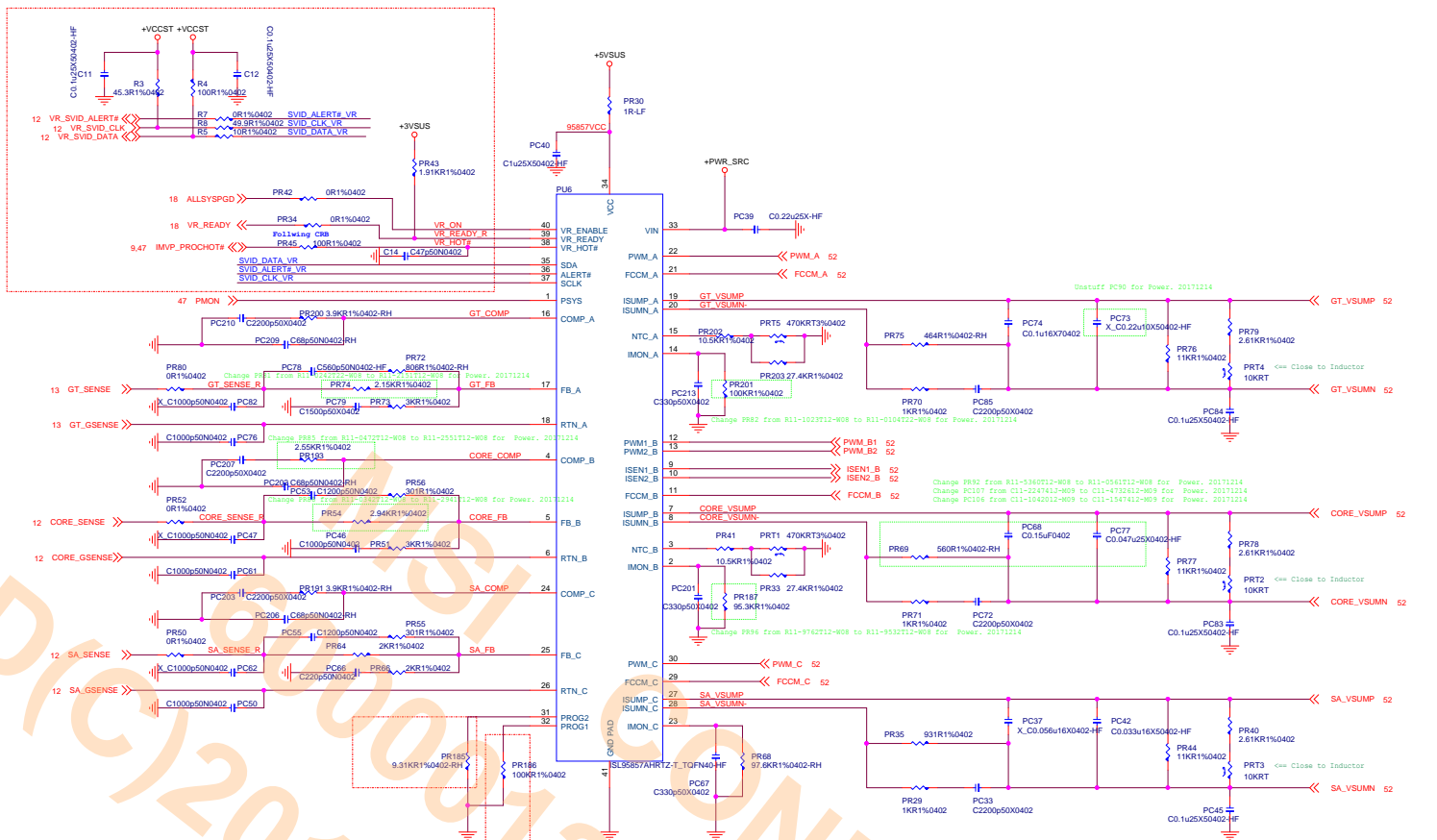
+1.8VRUN



+2.5V_MEM



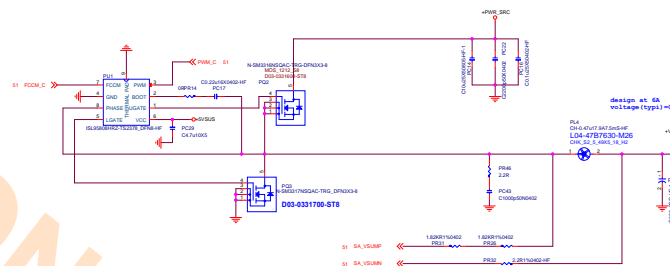
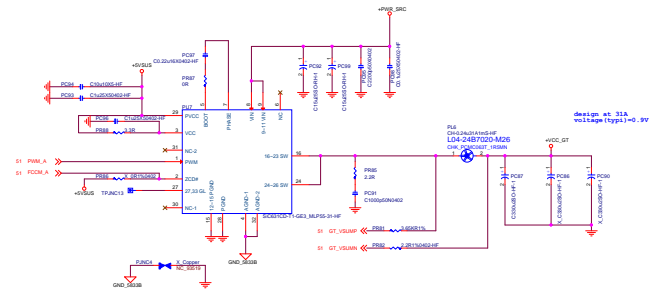
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Size	Document Number	Rev	
Custom	MS-14B2	10	
Date	Monday, May 28, 2018	Sheet	50 of 60



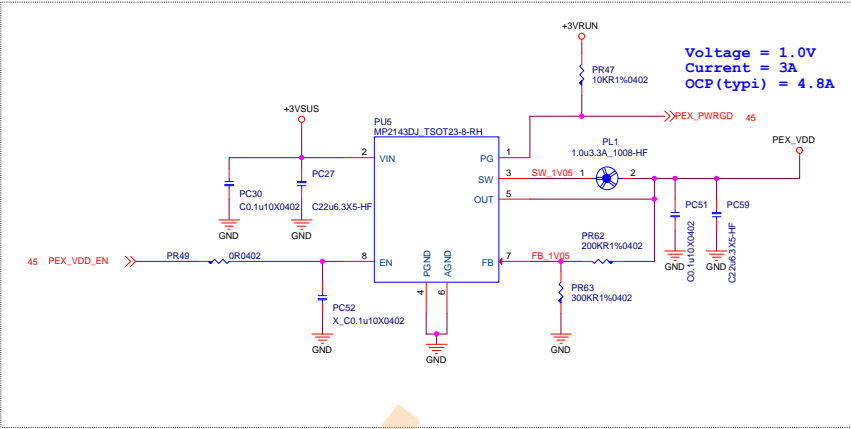
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File	+VCC CORE(1)		
Size	Document Number	MS-14B2	
Comp	Date	Monday, May 28, 2018	Sheet 51 of 60

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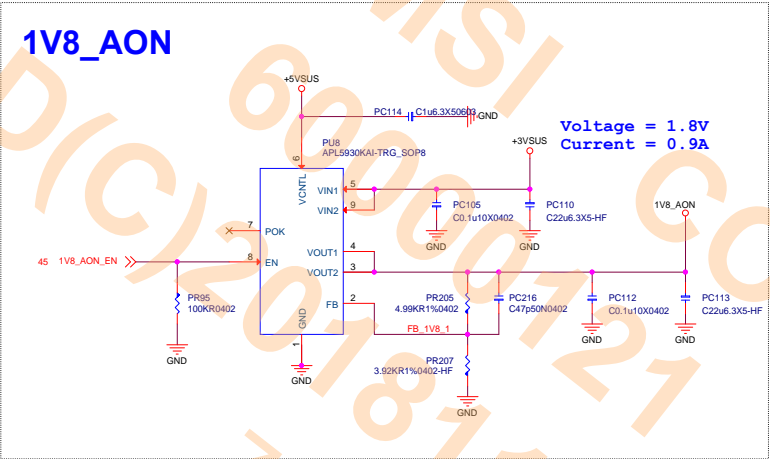
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PEX_VDD

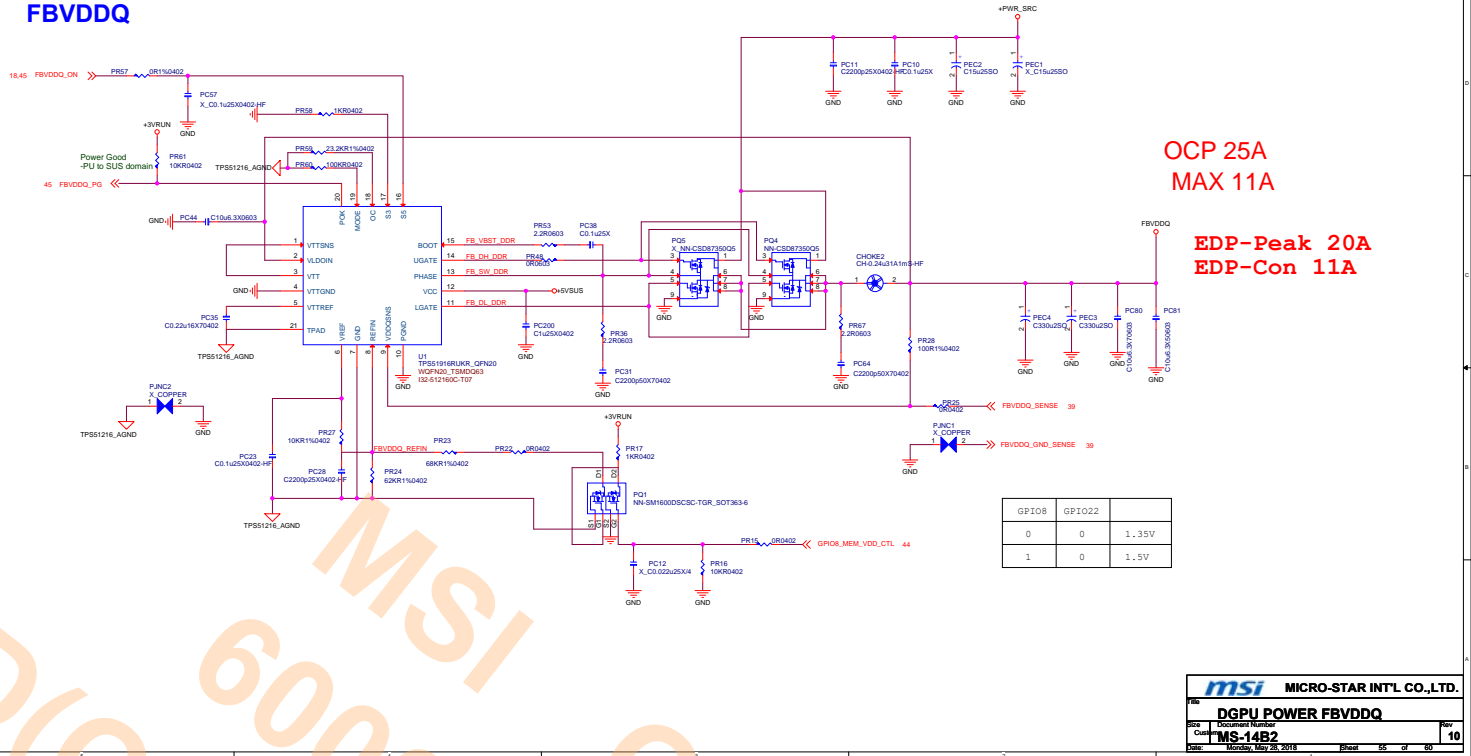


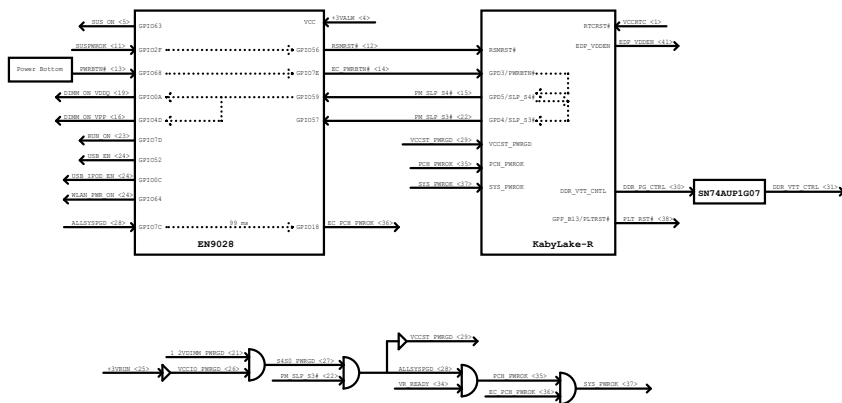
1V8_AON



msi		MICRO-STAR INT'L CO.,LTD.	
File		DGPU POWER PEX VDD/1V8 AON	
Size		Document Number	
Quality		MS-14B2	
Date		Monday, May 28, 2018	
		Sheet 53 of 60	
		Rev 10	

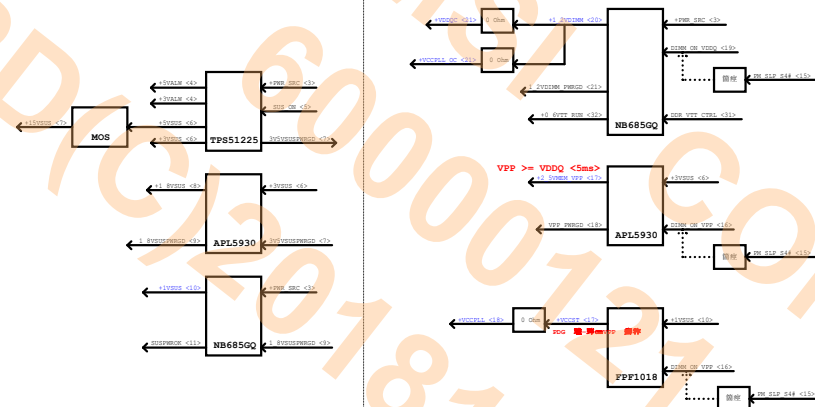
FBVDDQ



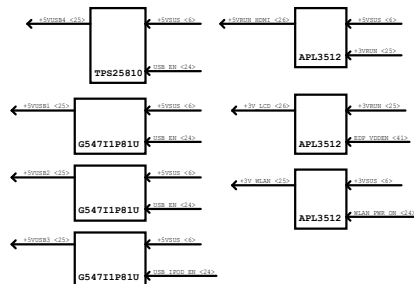
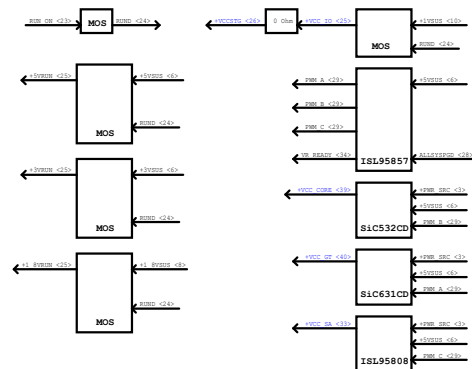


S4/S5

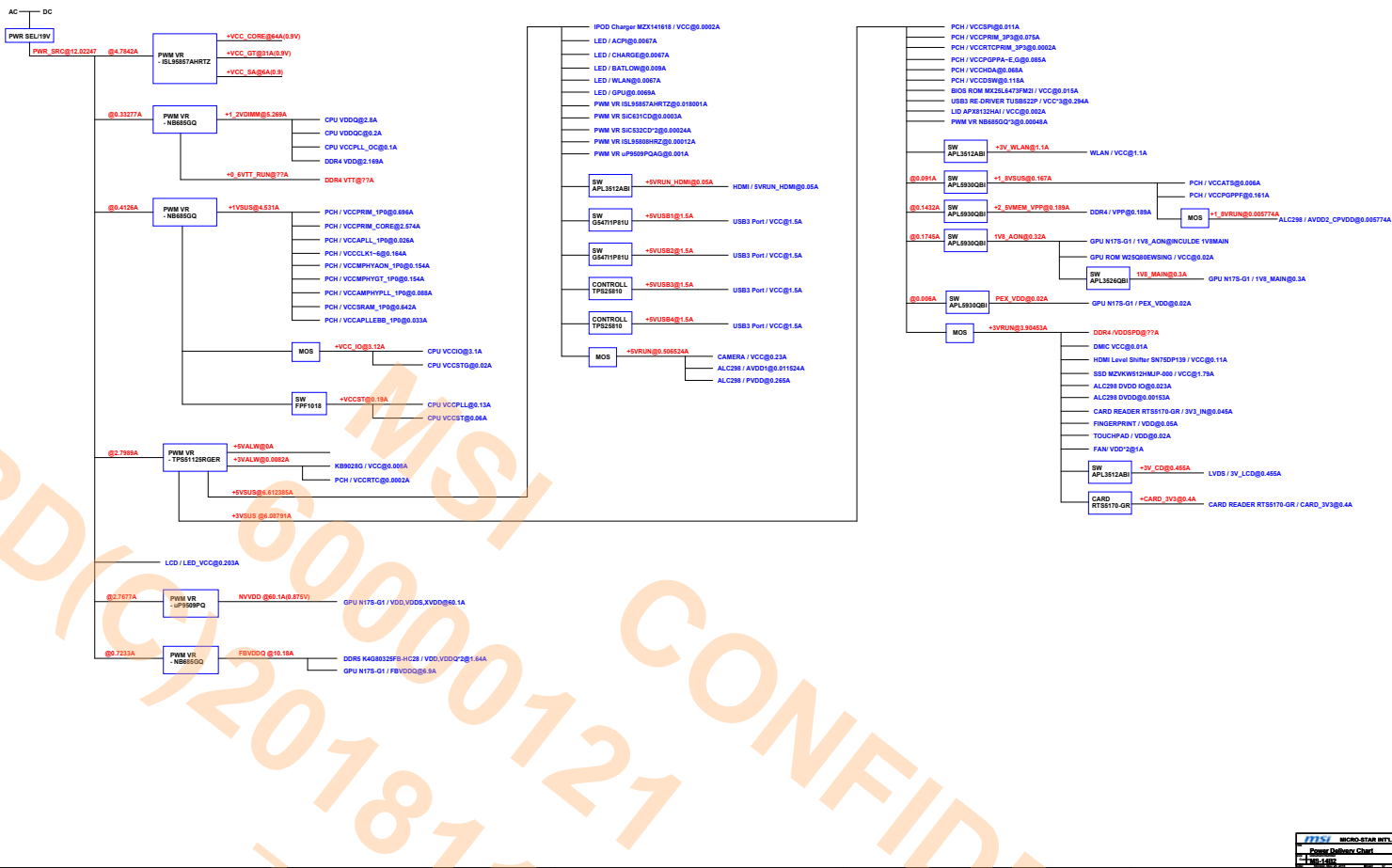
S3



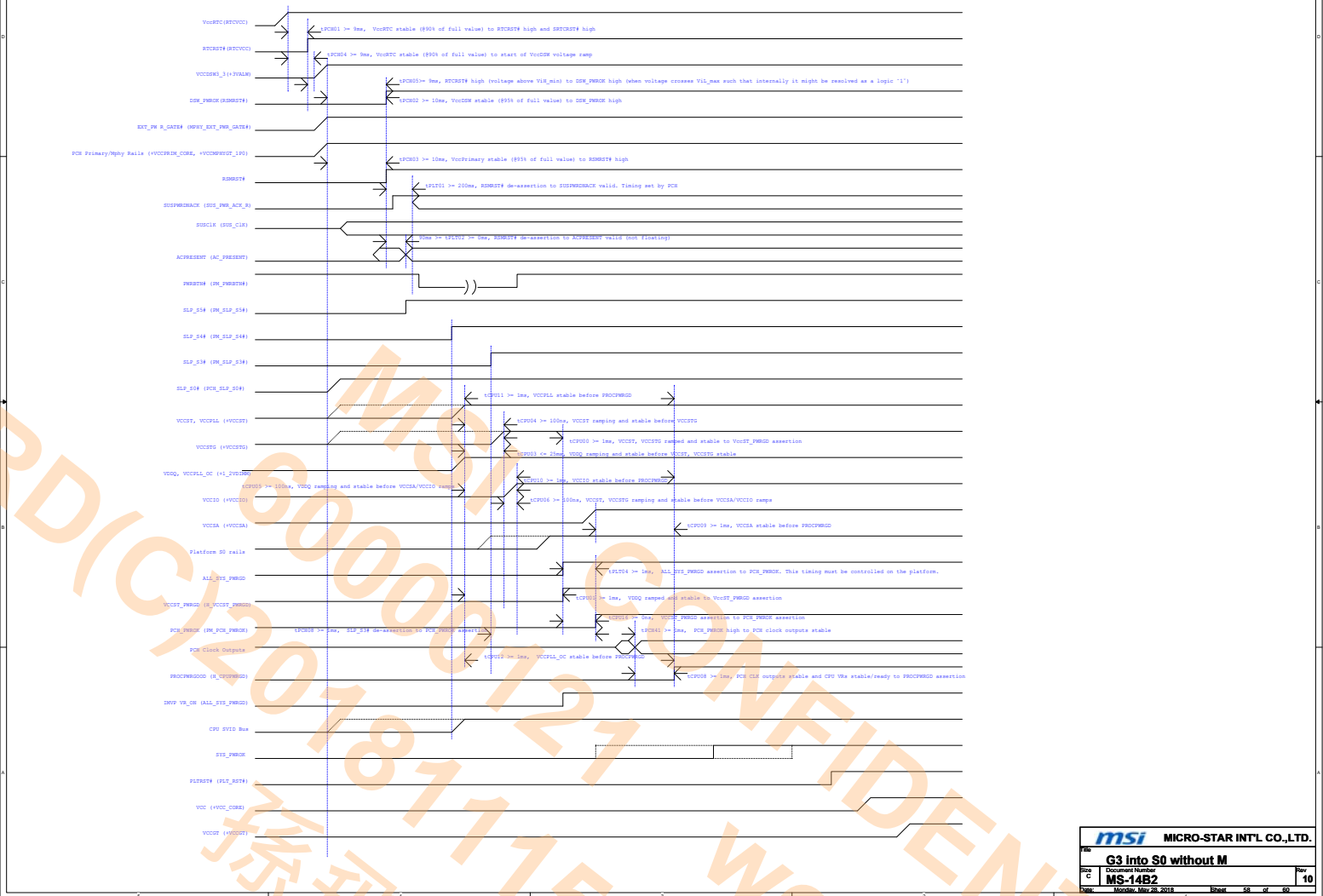
S0



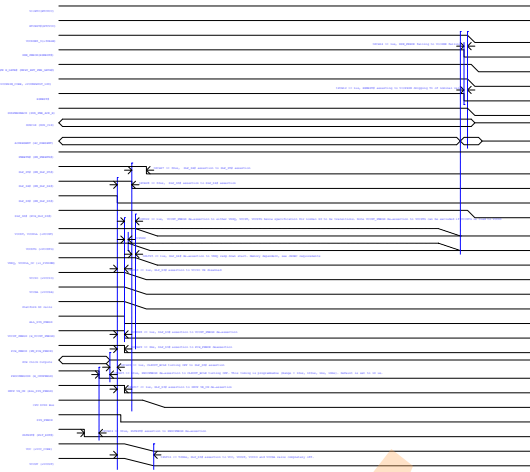
14B1 Power Delivery Chart



G3 to S0



S0 to G3



msi		MICRO-STAR INT'L CO.,LTD.	
File			
History			
Size	Document Number	Rev	
Customer	MS-14B2	10	
Date	Monday, May 28, 2018		
	Sheet	60	of 60